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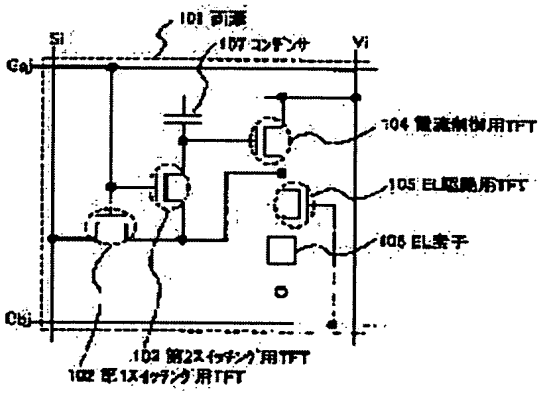
(54) LIGHT EMISSION DEVICE AND ITS DRIVING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide the driving method of a display device capable of obtaining constant luminance without being influenced by a change in the temperature.

SOLUTION: In this driving method, the change of luminance of an EL element due to temperature is prevented not by controlling a voltage to be applied to the EL element but by controlling a current flowing through the EL element. Concretely, a TFT controlling the current flowing through the EL element is made to be operated in the saturation region. Then, the current value IDS of the TFT is not almost changed by a VDS but it is decided only by a VGS. Thus, when the value of the VGS is determined so that the current value IDS becomes constant, the magnitude of the current flowing through the EL element becomes constant. Since the luminance of the element is roughly directly



proportional to the current flowing through the element, the change of the luminance of the element due to the temperature can be prevented.

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The 1st TFT, the 2nd TFT, the 3rd TFT, and the 4th TFT, It is luminescence equipment which has two or more pixels in which the EL element, the source signal line, and the current supply line were formed. Said the 3rd TFT and said 4th TFT The gate electrode is connected. Said the 3rd source field and drain field of TFT One side is connected to said source signal line, and another side is connected to the drain field of said 1st TFT. Said the 4th source field and drain field of TFT One side is connected to the drain field of said 1st TFT, and another side is connected to the gate electrode of said 1st TFT. It is luminescence equipment characterized by connecting the source field of said 1st TFT to said current supply line, connecting the drain field to the source field of said 2nd TFT, and connecting the drain field of said 2nd TFT to either of the two electrodes which said EL element has.
[Claim 2] The 1st TFT, the 2nd TFT, the 3rd TFT, and the 4th TFT, An EL element, a source signal line, the 1st gate signal line, and the 2nd gate signal line, It is luminescence equipment which has two or more pixels in which the current supply line was formed. Said the 3rd TFT and said 4th TFT Both gate electrodes are connected to said 1st gate signal line. Said the 3rd source field and drain field of TFT One side is connected to said source signal line, and another side is connected to the drain field of said 1st TFT. Said the 4th source field and drain field of TFT One side is connected to the drain field of said 1st TFT, and another side is connected to the gate electrode of said 1st TFT. The source field of said 1st TFT is connected to said current supply line, and the drain field is connected to the source field of said 2nd TFT. The drain field of said 2nd TFT It is luminescence equipment characterized by connecting with either of the two electrodes which said EL element has, and connecting the gate electrode of said 2nd TFT to said 2nd gate signal line.
[Claim 3] Luminescence equipment characterized by the polarity of said 3rd TFT and said 4th TFT being the same in claim 1 or claim 2.
[Claim 4] Are the drive approach of luminescence equipment of having two or more pixels in which TFT and an EL element were prepared, and said TFT is operating in the saturation region and is set at the 1st period. The magnitude of the current which flows to said channel formation field of TFT is controlled by the video signal, said VGS of TFT is controlled by said current, and it sets at the 2nd period. Said VGS of TFT is the drive approach of the luminescence equipment characterized by being held and a predetermined current flowing to said EL element through said TFT.
[Claim 5] Are the drive approach of luminescence equipment of having two or more pixels in which TFT and an EL element were prepared, and said TFT is operating in the saturation region and is set at the 1st period. The magnitude of the current which flows to said channel formation field of TFT is controlled by the video signal, said VGS of TFT is controlled by said current, and it sets at the 2nd period. The drive approach of luminescence equipment that the current which flows to said channel formation field of TFT by said VGS is characterized by flowing to said EL element.
[Claim 6] Are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, and an EL element were prepared, and said 1st TFT is

operating in the saturation region, and is set at the 1st period. The magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. VGS of said 1st TFT is the drive approach of the luminescence equipment characterized by being held and a predetermined current flowing to said EL element through said the 1st TFT and said 2nd TFT.
[Claim 7] Are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, and an EL element were prepared, and said 1st TFT is operating in the saturation region, and is set at the 1st period. The magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. The drive approach of luminescence equipment that the current which flows to the channel formation field of said 1st TFT by said VGS is characterized by flowing to said EL element through said 2nd TFT.
[Claim 8]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the EL panel which enclosed the EL element formed on the substrate between this substrate and covering material, and its drive approach. Moreover, it is related with EL module which mounted IC in this EL panel, and its drive approach. In addition, in this specification, an EL panel and EL module are named luminescence equipment generically. This invention relates to the electronic equipment using the luminescence equipment which displays by this drive approach further.
[0002]
[Description of the Prior Art] Since an EL element emits light itself, while its visibility is high, and it does not need a required back light with a liquid crystal display (LCD) but is the the best for thin-shape-izing, there is no limit also in an angle of visibility. Therefore, the luminescence equipment using an EL element attracts attention in recent years as a display which replaces CRT and LCD.
[0003] An EL element has the layer (it is hereafter described as EL layer) containing the organic compound with which the luminescence (Electro Luminescence) generated by adding electric field is obtained, an anode plate, and cathode. Although the luminescence in an organic compound has luminescence (phosphorescence) at the time of returning from luminescence at the time of returning from a singlet excitation state to a ground state (fluorescence), and a triplet excitation state to a ground state, which luminescence may be used with the luminescence equipment of this invention.
[0004] In addition, on these specifications, all the layers prepared between an anode plate and cathode are defined as EL layer. A luminous layer, a hole injection layer, an electronic injection layer, an electron hole transportation layer, an electron transport layer, etc. are concretely contained in EL layer. The EL element has fundamentally the structure where the laminating of an anode plate / luminous layer / the cathode was carried out to order, and, in addition to this structure, it may have the structure which carried out the laminating to order, such as an anode plate / hole injection layer / luminous layer / cathode, and an anode plate / hole injection layer / luminous layer / electron transport layer / cathode.
[0005] Moreover, in this specification, if an EL element drives that an EL element emits light, it will be called. Moreover, in this specification, the light emitting device formed in an anode plate, EL layer, and cathode is called an EL element.
[0006] By the way, the drive approach of luminescence equipment of having an EL element mainly has an analog drive and a digital drive. Especially, since it is possible to use the digital video signal (digital video signal) which has image information as it is, without changing into an analog, and to display an image corresponding to digitization of a broadcasting electric-wave, promising ** of the digital drive is carried out.
[0007] As an approach the binary electrical potential difference which a digital video signal has performs a gradation display, the surface-integral rate driving method and the time-sharing driving method are mentioned.
[0008] The surface-integral rate driving method is the driving method for performing a gradation

display by dividing 1 pixel into two or more sub-picture elements, and driving each sub-picture element based on a digital video signal independently. Since 1 pixel must be divided into two or more sub-picture elements and each sub-picture element is further driven independently, this surface-integral rate driving method needs to prepare the pixel electrode corresponding to each sub-picture element, respectively. Therefore, un-arranging [that the structure of a pixel becomes complicated] arises.

[0009] On the other hand, the time-sharing driving method is the driving method for performing a gradation display by controlling the die length which a pixel turns on. Specifically, an one-frame period is divided at two or more subframe periods. And in each subframe period, it is chosen whether each pixel lights up with a digital video signal or it does not carry out. The gradation of this pixel is called for in integrating the die length of the subframe period which the pixel turned on among all the subframe periods that appear during an one-frame period.

[0010] Generally, as for the organic electroluminescence ingredient, since the speed of response is quick compared with liquid crystal etc., the EL element fits the time-sharing drive.

[0011]

[Problem(s) to be Solved by the Invention] Below, the configuration of the pixel of the common luminescence equipment driven by time-sharing drive is explained using drawing 25 .

[0012] The circuit diagram of the pixel 9004 of the common luminescence equipment to drawing 25 is shown. The pixel 9004 has one of the source signal lines 9005, one of the current supply lines 9006, and one of the gate signal lines 9007. Moreover, the pixel 9004 has TFT9008 for switching, and TFT9009 for EL drive. The gate electrode of TFT9008 for switching is connected to the gate signal line 9007. As for the source field and drain field of TFT9008 for switching, one side is connected to the capacitor 9010 which the gate electrode and each pixel of TFT9009 for EL drive have [another side] in the source signal line 9005, respectively.

[0013] When TFT9008 for switching is in the condition (OFF state) of not choosing, the capacitor 9010 is formed in order to hold the gate voltage (potential difference between a gate electrode and a source field) of TFT9009 for EL drive.

[0014] Moreover, the source field of TFT9009 for EL drive is connected to the current supply line 9006, and a drain field is connected to EL element 9011. The current supply line 9006 is connected to the capacitor 9010.

[0015] EL element 9011 consists of an EL layer prepared between an anode plate, cathode, and an anode plate and cathode. When the anode plate has connected with the drain field of TFT9009 for EL drive, an anode plate turns into a pixel electrode and cathode turns into a counterelectrode. Conversely, when cathode has connected with the drain field of TFT9009 for EL drive, cathode turns into a pixel electrode and an anode plate turns into a counterelectrode.

[0016] Opposite potential is given to the counterelectrode of EL element 9011. Moreover, power-source potential is given to the current supply line 9006. Power-source potential and opposite potential are given according to the power source prepared in external IC of a display.

[0017] Next, actuation of the pixel shown in drawing 25 is explained.

[0018] By the selection signal inputted into the gate signal line 9007, TFT9008 for switching will be in the condition of ON, and the digital signal (it is hereafter called a digital video signal) which has the image information inputted into the source signal line 9005 will be inputted into the gate electrode of TFT9009 for EL drive through TFT9008 for switching.

[0019] Switching of TFT9009 for EL drive is controlled by information on 1 or 0 which the digital video signal inputted into the gate electrode of TFT9009 for EL drive has.

[0020] Since the potential of the current supply line 9006 is not given to the pixel electrode which EL element 9011 has when TFT9009 for EL drive becomes off, EL element 9011 does not emit light. Moreover, when TFT9009 for EL drive is turned on, the potential of the current supply line 9006 is given to the pixel electrode which EL element 9011 has, and EL element 9011 emits light.

[0021] An image is displayed by the above-mentioned actuation being performed in each pixel.

[0022] However, with the luminescence equipment which displays by the above-mentioned actuation, change of the temperature of EL layer which an EL element has with the heat which outside air temperature and the EL panel itself emit also changes the brightness of an EL

element in connection with the temperature change. Change of the volt ampere characteristic of an EL element when changing the temperature of EL layer to drawing 26 is shown. If the temperature of EL layer becomes low, the current which flows to an EL element will become small. On the contrary, if the temperature of EL layer becomes high, the current which flows to an EL element will become large.
[0023] As the current which flows to an EL element is small, the brightness of an EL element becomes lower. Moreover, as the current which flows to an EL element is large, the brightness of an EL element becomes higher. Therefore, since the magnitude of the current which flows in EL layer with temperature changes even when the electrical potential difference impressed to an EL element is fixed, the brightness of an EL element will also change.
[0024] Moreover, the rate of change of the brightness in a temperature change changes with EL ingredients. Therefore, in color display, when the EL element which has a different EL ingredient for every color is prepared, it may happen that a desired color is not obtained because the brightness of the EL element of each color changes with temperature scatteringly.
[0025] It asked for the design of the luminescence equipment which can obtain fixed brightness, without being influenced by the temperature change, and its drive approach in view of the problem mentioned above.
[0026]
[Means for Solving the Problem] this invention person is controlling by the current rather than controlling the brightness of an EL element by the electrical potential difference, and considered preventing change of the brightness of the EL element by temperature.
[0027] In order to pass a fixed current to an EL element, TFT which controls the magnitude of the current which flows to an EL element was operated in the saturation region, and this drain current of TFT was fixed. In addition, what is necessary is just to fill the following formulas 1, in order to operate TFT in a saturation region. However, VGS is the potential difference between a gate electrode and a source field, VTH is a threshold and VDS is the potential difference of a drain field and a source field.
[0028]
[Formula 1] | VGS-VTH|<|VDS| [0029] In the drain current (current value which flows to a channel formation field) and mu which are TFT about IDS, if the ratio of channel width W of a channel formation field and channel length L and VTH are made into a threshold and mu is made into mobility, the following formulas 2 will be realized [0 / mobility / of TFT /, and / C/ W/L / gate capacitance / per unit area /, and] in a saturation region.
[0030]
[Formula 2] IDS=mu C0 W/Lx(VGS-VTH)2/2[0031] As shown in a formula 2, in a saturation region, the drain current IDS hardly changes with VDS, but becomes settled only by VGS. Therefore, if the value of VGS is set that a current value IDS becomes fixed, the magnitude of the current which flows to an EL element will become fixed. Since the brightness of an EL element is mostly in direct proportion to the current which flows to an EL element, change of the brightness of the EL element by temperature can be prevented.
[0032] Below, the configuration of this invention is shown.
[0033] By this invention, the 1st TFT, the 2nd TFT, and the 3rd TFT, It is luminescence equipment which has two or more pixels in which the 4th TFT, EL element, source signal line, and current supply line were formed. Said the 3rd TFT and said 4th TFT The gate electrode is connected. Said the 3rd source field and drain field of TFT One side is connected to said source signal line, and another side is connected to the drain field of said 1st TFT. Said the 4th source field and drain field of TFT One side is connected to the drain field of said 1st TFT, and another side is connected to the gate electrode of said 1st TFT. The source field of said 1st TFT is connected to said current supply line, and the drain field is connected to the source field of said 2nd TFT. The drain field of said 2nd TFT The luminescence equipment characterized by connecting with either of the two electrodes which said EL element has is offered.
[0034] By this invention, the 1st TFT, the 2nd TFT, and the 3rd TFT, The 4th TFT, an EL element, a source signal line, and the 1st gate signal line, It is luminescence equipment which has two or more pixels in which the 2nd gate signal line and current supply line were formed. Said the

3rd TFT and said 4th TFT Both gate electrodes are connected to said 1st gate signal line. Said the 3rd source field and drain field of TFT One side is connected to said source signal line, and another side is connected to the drain field of said 1st TFT. Said the 4th source field and drain field of TFT One side is connected to the drain field of said 1st TFT, and another side is connected to the gate electrode of said 1st TFT. The source field of said 1st TFT is connected to said current supply line, and the drain field is connected to the source field of said 2nd TFT. The drain field of said 2nd TFT It connects with either of the two electrodes which said EL element has, and the luminescence equipment characterized by connecting the gate electrode of said 2nd TFT to said 2nd gate signal line is offered.

[0035] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which TFT and an EL element were prepared, and said TFT is operating in the saturation region and is set at the 1st period. The magnitude of the current which flows to said channel formation field of TFT is controlled by the video signal, said VGS of TFT is controlled by said current, and it sets at the 2nd period. The drive approach of the luminescence equipment characterized by holding said VGS of TFT and a predetermined current flowing to said EL element through said TFT is offered.

[0036] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which TFT and an EL element were prepared, and said TFT is operating in the saturation region and is set at the 1st period. The magnitude of the current which flows to said channel formation field of TFT is controlled by the video signal, said VGS of TFT is controlled by said current, and it sets at the 2nd period. The drive approach of luminescence equipment that the current which flows to said channel formation field of TFT by said VGS is characterized by flowing to said EL element is offered.

[0037] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, and an EL element were prepared, and said 1st TFT is operating in the saturation region, and is set at the 1st period. The magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. The drive approach of the luminescence equipment characterized by holding VGS of said 1st TFT and a predetermined current flowing to said EL element through said the 1st TFT and said 2nd TFT is offered.

[0038] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, and an EL element were prepared, and said 1st TFT is operating in the saturation region, and is set at the 1st period. The magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. The drive approach of luminescence equipment that the current which flows to the channel formation field of said 1st TFT by said VGS is characterized by flowing to said EL element through said 2nd TFT is offered.

[0039] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which TFT and an EL element were prepared, and said TFT is operating in the saturation region and is set at the 1st period. The magnitude of the current which flows to said channel formation field of TFT is controlled by the video signal, said VGS of TFT is controlled by said current, and it sets at the 2nd period. Said VGS of TFT is held, and a predetermined current flows to said EL element through said TFT, and the drive approach of the luminescence equipment characterized by a current not flowing to said EL element in the 3rd period is offered.

[0040] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which TFT and an EL element were prepared, and said TFT is operating in the saturation region and is set at the 1st period. The magnitude of the current which flows to said channel formation field of TFT is controlled by the video signal, said VGS of TFT is controlled by said current, and it sets at the 2nd period. The drive approach of the luminescence equipment characterized by for the current which flows to said channel formation field of TFT flowing to said EL element, and a current not flowing to said EL element in the 3rd period by said VGS is offered.

[0041] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, and an EL element were prepared, and said 1st TFT is operating in the saturation region, and is set at the 1st period. The magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. VGS of said 1st TFT is held, and a predetermined current flows to said EL element through said the 1st TFT and said 2nd TFT, and the drive approach of the luminescence equipment characterized by said 2nd TFT becoming off is offered in the 3rd period.
[0042] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, and an EL element were prepared, and said 1st TFT is operating in the saturation region, and is set at the 1st period. The magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. The current which flows to the channel formation field of said 1st TFT by said VGS flows to said EL element through said 2nd TFT, and the drive approach of the luminescence equipment characterized by said 2nd TFT becoming off is offered in the 3rd period.
[0043] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, the 3rd TFT, the 4th TFT, and an EL element were prepared, and it sets at the 1st period. Said the 1st gate electrode and drain field of TFT are connected by said the 3rd TFT and said 4th TFT. And the magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. The drive approach of the luminescence equipment characterized by holding VGS of said 1st TFT and a predetermined current flowing to said EL element through said 1st TFT is offered.
[0044] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, the 3rd TFT, the 4th TFT, and an EL element were prepared, and it sets at the 1st period. Said the 1st gate electrode and drain field of TFT are connected by said the 3rd TFT and said 4th TFT. And the magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. The drive approach of luminescence equipment that the current which flows to the channel formation field of said 1st TFT by said VGS is characterized by flowing to said EL element through said 2nd TFT is offered.

[0045] By this invention, the 1st TFT, the 2nd TFT, and the 3rd TFT, Are the drive approach of luminescence equipment of having two or more pixels in which the 4th TFT and an EL element were prepared, fixed potential is given to the source field of said 1st TFT, and it sets at the 1st period. Through said the 3rd TFT and said 4th TFT, a video signal is inputted into said the 1st gate electrode and drain field of TFT, and it sets at the 2nd period. The drive approach of the luminescence equipment characterized by a predetermined current flowing to said EL element through said the 1st TFT and said 2nd TFT with the potential of said video signal is offered.
[0046] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, the 3rd TFT, the 4th TFT, and an EL element were prepared, and it sets at the 1st period. Said the 1st gate electrode and drain field of TFT are connected by said the 3rd TFT and said 4th TFT. And the magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said 1st TFT is controlled by said current, and it sets at the 2nd period. VGS of said 1st TFT is held, and a predetermined current flows to said EL element through said 1st TFT, and the drive approach of the luminescence equipment characterized by said 2nd TFT becoming off is offered in the 3rd period.
[0047] By this invention, are the drive approach of luminescence equipment of having two or more pixels in which the 1st TFT, the 2nd TFT, the 3rd TFT, the 4th TFT, and an EL element were prepared, and it sets at the 1st period. Said the 1st gate electrode and drain field of TFT are connected by said the 3rd TFT and said 4th TFT. And the magnitude of the current which flows to the channel formation field of said 1st TFT is controlled by the video signal, VGS of said

1st TFT is controlled by said current, and it sets at the 2nd period. The current which flows to the channel formation field of said 1st TFT by said VGS flows to said EL element through said 2nd TFT, and the drive approach of the luminescence equipment characterized by said 2nd TFT becoming off is offered in the 3rd period.
[0048] By this invention, the 1st TFT, the 2nd TFT, and the 3rd TFT, Are the drive approach of luminescence equipment of having two or more pixels in which the 4th TFT and an EL element were prepared, fixed potential is given to the source field of said 1st TFT, and it sets at the 1st period. Through said the 3rd TFT and said 4th TFT, a video signal is inputted into said the 1st gate electrode and drain field of TFT, and it sets at the 2nd period. With the potential of said video signal, through said the 1st TFT and said 2nd TFT, a predetermined current flows to said EL element, and the drive approach of the luminescence equipment characterized by said 2nd TFT becoming off is offered in the 3rd period.
[0049] This invention may be characterized by the polarity of said 3rd TFT and said 4th TFT being the same.
[0050]
[Embodiment of the Invention] (Gestalt 1 of operation) The configuration of the pixel of this invention is shown in drawing 1 .
[0051] The pixel 101 shown in drawing 1 has the source signal line Si (1 of S1-Sx(es)), the gate signal line Gaj for writing (1 of Ga1-Gay(s)), the gate signal line Gbj (1 of Gb1-Gb(ies)) for a display, and the current supply line Vi (1 of V1-Vx(es)).
[0052] In addition, the number of a source signal line and current supply lines is not necessarily the same. Moreover, the number of the gate signal line for writing and the gate signal lines for a display is not necessarily the same. Moreover, it is not necessary to surely have these wiring altogether, and another different wiring may be prepared besides these wiring.
[0053] Moreover, the pixel 101 has TFT102 for the 1st switching, TFT103 for the 2nd switching, TFT104 for current control, TFT105 for EL drive, EL element 106, and the capacitor 107.
[0054] Both the gate electrodes of TFT102 for the 1st switching and TFT103 for the 2nd switching are connected to the gate signal line Gaj for writing.
[0055] In addition, electric connection is meant as long as connection is unstated especially in this specification.
[0056] One side is connected to the source signal line Si, and another side is connected to the source field of TFT105 for EL drive for the source field and drain field of TFT102 for the 1st switching. Moreover, one side is connected to the source field of TFT105 for EL drive, and another side is connected to the gate electrode of TFT104 for current control for the source field and drain field of TFT103 for the 2nd switching.
[0057] That is, either [the source field of TFT103 for the 2nd switching and a drain field] the source field of TFT102 for the 1st switching or the drain field is connected.
[0058] The source field of TFT104 for current control is connected to the current supply line Vi, and the drain field is connected to the source field of TFT105 for EL drive.
[0059] In addition, let the electrical potential difference which the source field of an n channel mold transistor is given be a thing lower than the electrical potential difference given to a drain field on these specifications. Moreover, let the electrical potential difference which the source field of a p channel mold transistor is given be a thing higher than the electrical potential difference given to a drain field.
[0060] The gate electrode of TFT105 for EL drive is connected to the gate signal line Gbj for a display. And the drain field of TFT105 for EL drive is connected to the pixel electrode which EL element 106 has. EL element 106 has EL layer prepared between the pixel electrode, the counterelectrode, and a pixel electrode and a counterelectrode. The counterelectrode of EL element 106 is connected to the power source (power source for counterelectrodes) prepared in the exterior of an EL panel.
[0061] The potential (power-source potential) of the current supply line Vi is maintained at fixed height. Moreover, the potential of the power source for counterelectrodes is also maintained at fixed height.
[0062] In addition, either the n channel mold TFT or the p channel mold TFT is OK as TFT102

for the 1st switching, and TFT103 for the 2nd switching. However, the polarity of TFT102 for the 1st switching and TFT103 for the 2nd switching is the same.
[0063] Moreover, either the n channel mold TFT or the p channel mold TFT is OK as TFT104 for current control.
[0064] Either the n channel mold TFT or the p channel mold TFT is OK as TFT105 for EL drive. One side is an anode plate and another side of the pixel electrode and counterelectrode of an EL element is cathode. When cathode is used as a counterelectrode, using an anode plate as a pixel electrode, as for TFT105 for EL drive, it is desirable that it is the p channel mold TFT. On the contrary, when using an anode plate as a counterelectrode, using cathode as a pixel electrode, as for TFT105 for EL drive, it is desirable that it is the n channel mold TFT.
[0065] The capacitor 107 is formed between the gate electrode of TFT104 for current control, and the source field. Although it is prepared in order to maintain more certainly the electrical potential difference (VGS) between the gate electrode of TFT104 for current control, and a source field when TFT 102 and 103 for the 1st and 2nd switching is OFF, it is not necessary to necessarily form a capacitor 107.
[0066] Drawing 2 is the block diagram of the luminescence equipment which uses the drive approach of this invention, and, for 100, as for a source signal-line drive circuit and 111, a picture element part and 110 are [the gate signal line drive circuit for writing and 112] the gate signal line drive circuits for a display.
[0067] The picture element part 100 has the source signal lines S1-Sx, the gate signal lines Ga1-Gay for writing, the gate signal lines Gb1-Gby for a display, and the current supply lines V1-Vx.
[0068] The field which has a source signal line, the gate signal line for writing, a gate signal line for a display, and every one current supply line, respectively is a pixel 101. Two or more pixels 101 are formed in the shape of a matrix at the picture element part 100.
[0069] (Gestalt 2 of operation) The drive of the luminescence equipment of this invention shown in 5272 next drawing 1 , and drawing 2 is explained using drawing 3 . The drive of the luminescence equipment of this invention can be divided and explained at the write-in period Ta and the display period Td.
[0070] The timing chart of the signal inputted into the gate signal line for writing and the gate signal line for a display in the write-in period Ta at drawing 3 (A) is shown. ON shows the period when the gate signal line for writing and the gate signal line for a display are chosen, and the period which in other words has all TFT(s) by which the gate electrode is connected to this signal line in the condition of ON. On the contrary, OFF shows the period when the gate signal line for writing and the gate signal line for a display are not chosen, and the period which in other words has all TFT(s) by which the gate electrode is connected to this signal line in an off condition.
[0071] In the write-in period Ta, the gate signal lines Ga1-Gay for writing are chosen in order, and the gate signal lines Gb1-Gby for a display are not chosen. And it is chosen as each of the source signal lines S1-Sx by the digital video signal inputted into the source signal-line drive circuit 110 whether the fixed current Ic flows or it does not flow.
[0072] The schematic diagram which is a pixel when the fixed current Ic flows is shown in the source signal line Si in the write-in period Ta at drawing 4 (A). Since TFT102 for the 1st switching and TFT103 for the 2nd switching are in the condition of ON, if the fixed current Ic flows to the source signal line Si, the fixed current Ic will flow between the drain field of TFT104 for current control, and a source field.
[0073] It connects with the current supply line Vi, and the source field of TFT104 for current control is maintained at fixed potential (power-source potential).
[0074] Since TFT104 for current control is operating in the saturation region, if Ic is substituted for IDS of a formula 2, the value of VGS will become settled naturally.
[0075] In addition, when the fixed current Ic does not flow to the source signal line Si, the source signal line Si is maintained at the same potential as the current supply line Vi. Therefore, it is set to VGS**0 in this case.
[0076] Termination of the write-in period Ta starts the display period Td.

[0077] The timing chart of the signal inputted into the gate signal line for writing and the gate signal line for a display in the display period Td at drawing 3 (B) is shown.
[0078] In the display period Td, the gate signal lines Ga1-Gay for writing are not chosen altogether, but the gate signal lines Gb1-Gby for a display are chosen altogether.
[0079] The schematic diagram of the pixel in the display period Td is shown in drawing 4 (B). TFT102 for the 1st switching and TFT103 for the 2nd switching are in an off condition. Moreover, it connects with the current supply line Vi, and the source field of TFT104 for current control is maintained at fixed potential (power-source potential).
[0080] In the display period Td, VGS defined in the write-in period Ta is maintained. Therefore, if the value of VGS is assigned to a formula 2, the value of IDS will become settled naturally.
[0081] Since it is VGS**0 when Current Ic does not flow in the write-in period Ta, when a threshold is 0, a current does not flow. Therefore, EL element 106 does not emit light.
[0082] If the value of VGS is assigned to a formula 2 when the fixed current Ic flows in the write-in period Ta, Ic will be obtained as a current value IDS. Since TFT105 for EL drive is turned on in the display period Td, Current Ic flows to EL element 106, and EL element 106 emits light.
[0083] As mentioned above, it is possible to display one image by writing in during an one-frame period and repeating Period Ta and the display period Td. When displaying an image with a n-bit digital video signal, at least n write-in periods and n display periods are established within an one-frame period.
[0084] n write-in periods (Ta1-Tan) and n display periods (Td1-Tdn) support each bit of a digital video signal.
[0085] The timing to which n write-in periods (Ta1-Tan) and n display periods (Td1-Tdn) appear in drawing 5 in an one-frame period is shown. The axis of abscissa shows time amount and the axis of ordinate shows the location of the gate signal line for writing which a pixel has, and the gate signal line for a display.
[0086] Tdm appears at the degree of the write-in period Tam (the number of the arbitration of m1-n) in the display period corresponding to the same number of bits, and this case. The write-in period Ta and the display period Td are doubled, and it is called the subframe period SF. The subframe period which has the write-in period Tam corresponding to the m-th bit and the display period Tdm serves as SFm.
[0087] The die length of the display periods Td1-Tdn is Td1:Td2. : -- It is :Tdn=20:21. : -- :2n-1 is filled.
[0088] Gradation is expressed as the drive approach of this invention by controlling the sum of the die length of the display period in an one-frame period which emits light.
[0089] By the configuration mentioned above, the luminescence equipment of this invention can obtain fixed brightness, without being influenced by the temperature change. Moreover, in color display, even when the EL element which has a different EL ingredient for every color is prepared, the brightness of the EL element of each color can prevent changing scatteringly and not obtaining a desired color with temperature.
[0090] (Gestalt 3 of operation) The drive approach which is different in the gestalt 2 of operation of the luminescence equipment of this invention shown in 5318 next drawing 1 , and drawing 2 is explained using drawing 6 -9.
[0091] In the pixel of the 1st line, the write-in period Ta 1 is started first.
[0092] In the write-in period Ta 1, the gate signal line Ga1 for writing is chosen from the gate signal line drive circuit 111 for writing by the 1st selection signal (selection signal for writing) inputted into the gate signal line Ga1 for writing. In addition, it means that all TFT(s) by which the gate electrode is connected to this signal line as a signal line is chosen in this specification will be in the condition of ON. And TFT102 for the 1st switching and TFT103 for the 2nd switching of all pixels (the pixel of the 1st line) which have the gate signal line Ga1 for writing will be in the condition of ON.
[0093] Moreover, in the write-in period Ta 1, the gate signal line Gb1 for a display which the pixel of the 1st line has is not chosen. Therefore, TFT105 for EL drive which the pixel of the 1st line has is in the off condition altogether.

[0094] And the value of the current which flows to the source signal lines S1-Sx is defined by the bit [1st] digital video signal inputted into the source signal-line drive circuit 110.
[0095] A digital video signal has the information on "0" or "1", and is. The digital video signal which has the information on "0", and the digital video signal which has the information on "1" are signals with which one side has Hi (High) and one side has the electrical potential difference of Lo (Low). The value of the drain current which flows to TFT104 for current control is controlled by information on "0" or "1" which a digital video signal has.
[0096] Specifically, it is chosen whether the fixed current Ic flows between the current supply line Vi and the source signal line Si using "0" of a digital video signal or the information on "1" through TFT104 for current control, TFT102 for the 1st switching, and TFT103 for the 2nd switching or a current does not flow.
[0097] In addition, that the digital video signal was inputted into the pixel in this specification means that it is chosen whether the fixed current Ic flows [this pixel] between the current supply line Vi and the source signal line Si with a digital video signal or a current does not flow.
[0098] The schematic diagram of the pixel in the write-in period Ta 1 is shown in drawing 8 (A).
[0099] In the write-in period Ta 1, the gate signal line Gb1 for selection and a display has the gate signal line Ga1 for writing in the condition of not choosing. Therefore, since TFT102 for the 1st switching and TFT103 for the 2nd switching are turned on, if the fixed current Ic flows to the source signal line Si, the fixed current Ic will flow between the source field of TFT for current control, and a drain field. And since TFT105 for EL drive is off at this time, the potential of the current supply line Vi is not given to the pixel electrode of EL element 106, but EL element 106 is in a nonluminescent condition.
[0100] It connects with the current supply line Vi, and the source field of TFT104 for current control is maintained at fixed potential (power-source potential). Moreover, since TFT104 for current control is operating in the saturation region, if Ic is substituted for IDS of a formula 2, the value of VGS of TFT104 for current control will become settled naturally.
[0101] The fixed current Ic flows to the source signal line Si, it is in it inside, and the case is maintained at the potential with same source signal line Si and current supply line Vi. In this case, TFT104 for current control is set to VGS**0.
[0102] And after selection of the gate signal line Ga1 for writing is completed, it writes in in the pixel of the 1st line and a period Ta 1 expires.
[0103] After it writes in in the pixel of the 1st line and a period Ta 1 expires, it writes in in the pixel of the 2nd line and a period Ta 1 is started. And by the selection signal for writing, the gate signal line Ga2 for writing is chosen, and the same actuation as the pixel of the 1st line is performed. And the gate signal lines Ga3-Gay for writing are also chosen in order, and are written in in all pixels, a period Ta 1 is started, and the same actuation as the pixel of the 1st line is performed.
[0104] The timing which appears by the pixel of each Rhine differs, and the write-in period Ta 1 is equivalent to the period when the gate signal line for writing which the pixel of each Rhine has is chosen. The timing by which the write-in period Ta is started has time difference for every pixel of each Rhine, respectively.
[0105] On the other hand, after it writes in in the pixel of the 1st line and a period Ta 1 expires, a concurrency is carried out to writing in in the pixel of Rhine after the 2nd line, and a period Ta 1 being started, and the display period Tr1 is started in the pixel of the 1st line.
[0106] In the display period Tr1, the gate signal line Gb1 for a display is chosen from the gate signal line drive circuit 112 for a display by the 2nd selection signal (selection signal for a display) inputted into the gate signal line Gb1 for a display. Selection is started before selection of the gate signal lines Ga2-Gay for writing ends the gate signal line Gb1 for a display. It is good to start selection of the gate signal line Gb1 for a display at the same time selection of the gate signal line Ga1 for writing is completed and selection of the gate signal line Ga2 for writing is started more preferably.
[0107] The schematic diagram of the pixel in the display period Tr1 is shown in drawing 8 (B).
[0108] In the display period Tr1, the gate signal line Gb1 for un-choosing and a display has the gate signal line Ga1 for writing in the condition of selection. Therefore, in the pixel of the 1st line,

TFT102 for the 1st switching and TFT103 for the 2nd switching are off, and TFT105 for EL drive is turned on.
[0109] It connects with the current supply line Vi, and the source field of TFT104 for current control is maintained at fixed potential (power-source potential). And VGS of TFT104 for current control defined in the write-in period Ta 1 is maintained by the capacitor 107 etc., even after selection of the gate signal line Ga1 for writing is completed. The current IDS which flows between the source field of TFT104 for current control and a drain field at this time is searched for by assigning the value of VGS to a formula 2. Current IDS flows to EL element 106 through TFT105 for EL drive of ON, and, as a result, EL element 106 emits light.
[0110] When the gate signal line Ga1 for writing is chosen and Current Ic does not flow, it is VGS**0 of TFT104 for current control. Therefore, a current does not flow between the source field of TFT104 for current control, and a drain field. Therefore, EL element 106 does not emit light.
[0111] Thus, after a digital video signal is inputted into a pixel, by the gate signal line for a display being chosen, EL element 106 will be in luminescence or a nonluminescent condition, and a pixel will display.
[0112] After the display period Tr1 is started in the pixel of the 1st line, the display period Tr1 is started also in the pixel of the 2nd line. And by the selection signal for a display, the gate signal line Gb2 for a display is chosen, and the same actuation as the pixel of the 1st line is performed. And the gate signal lines Gb3-Gby for a display are also chosen in order, the display period Tr1 is started in all pixels, and the same actuation as the pixel of the 1st line is performed.
[0113] The display period Tr1 of the pixel of each Rhine is equivalent to the period when the gate signal line for a display which the pixel of each Rhine has is chosen. The timing by which the display period Tr is started has time difference for every pixel of each Rhine, respectively.
[0114] On the other hand, a concurrency is carried out to the display period Tr1 being started in the pixel of Rhine after the 2nd line, selection of the gate signal line Gb1 for a display is completed in the pixel of the 1st line, and the display period Tr1 expires.
[0115] In the pixel of the 1st line, termination of the display period Tr1 starts the non-display period Td1. And the gate signal line Gb1 for a display will be in the condition of not choosing, and TFT105 for EL drive of the pixel of the 1st line will become off. At this time, the gate signal line Ga1 for writing is still the condition of not choosing.
[0116] Since TFT105 for EL drive becomes off in the pixel of the 1st line, EL element 106 to which the power-source potential of the current supply line Vi will not be given to the pixel electrode of EL element 106 and which the pixel of the 1st line has will be in a nonluminescent condition altogether, and the pixel of the 1st line will stop displaying therefore.
[0117] The schematic diagram which is the pixel of the 1st line when the gate signal line Gb1 for a display and the gate signal line Ga1 for writing are not chosen as drawing 8 (C) is shown. TFT102 for the 1st switching and TFT103 for the 2nd switching are off, and TFT105 for EL drive is also off. Therefore, EL element 106 is in the nonluminescent condition.
[0118] After the non-display period Td1 is started in the pixel of the 1st line, the display period Tr1 expires also in the pixel of the 2nd line, and the non-display period Td1 is started. And by the selection signal for a display, the gate signal line Gb2 for a display is chosen, and the same actuation as the pixel of the 1st line is performed in the pixel of the 2nd line. And the gate signal lines Gb3-Gby for a display are also chosen in order, the display period Tr1 ends them in all pixels, the non-display period Td1 is started, and the same actuation as the pixel of the 1st line is performed.
[0119] the timing by which the non-display period Td1 is started has time difference by the pixel of each Rhine, and the gate signal line for writing which the pixel of each Rhine has chooses the non-display period Td1 — not having -- in addition -- and it is equivalent to the period when the gate signal line for a display is chosen.
[0120] On the other hand, after the non-display period Td1 is started in that the non-display period Td1 is started in the pixel of Rhine after the 2nd line, a concurrency, or all pixels, in the pixel of the 1st line, selection of the gate signal line Ga1 for writing is started, and the write-in period Ta 2 is started.

[0121] In addition, in this invention, since the write-in period of the pixel of each Rhine does not lap mutually, after the write-in period in the pixel of the y-th line expires, the write-in period in the pixel of the 1st line is started.
[0122] Actuation of a pixel is the same as that of the case of the write-in period Ta 1. However, the bit [2nd] digital video signal is inputted into a pixel in the write-in period Ta 2.
[0123] And after it writes in in the pixel of the 1st line and a period Ta 2 expires, next, in the pixel after the 2nd line, it writes in in order and a period Ta 2 is started.
[0124] A concurrency is carried out to writing in in the pixel after the 2nd line and a period Ta 2 being started, and the display period Tr2 is started in the pixel of the 1st line. Also in the display period Tr2, a pixel displays with the bit [2nd] digital video signal like the display period Tr1.
[0125] And after the display period Tr1 is started in the pixel of the 1st line, also in the pixel after the 2nd line, it writes in in order, a period Ta 2 expires, and the display period Tr2 is started. Therefore, the pixel of each Rhine displays.
[0126] On the other hand, a concurrency is carried out to the display period Tr2 being started in the pixel of Rhine after the 2nd line, the display period Tr2 expires in the pixel of the 1st line, and the non-display period Td2 is started. ** [initiation of the non-display period Td2 / stop / a pixel / displaying in the pixel of the 1st line]
[0127] After the non-display period Td2 is started in the pixel of the 1st line, also in the pixel after the 2nd line, the display period Tr2 expires in order, and the non-display period Td2 is started. A pixel stops and displaying in each Rhine.
[0128] Before the bit [m-th] digital video signal is inputted into a pixel, as for the actuation mentioned above, the write-in period Ta, the display period Tr, and the non-display period Td appear repeatedly for every line crack and pixel of each Rhine.
[0129] Signs that the gate signal lines Ga1-Gay for writing and the gate signal lines Gb1-Gby for a display are chosen as drawing 6 in the write-in period Ta 1, the display period Tr1, and the non-display period Td1 are shown.
[0130] For example, if the pixel of the 1st (First Line) line is observed, a pixel will not display in the write-in period Ta 1 and the non-display period Td1. And it is displaying only in the display period Tr1. In addition, in drawing 6 , in order to write in and to explain actuation of the pixel in Periods Ta1-Ta (m-1), the display periods Tr1-Tr (m-1), and the non-display periods Td1-Td (m-1), actuation of the pixel in the write-in period Ta 1, the display period Tr1, and the non-display period Td1 is illustrated. Therefore, no pixel of Rhine displays in the write-in periods Ta1-Ta (m-1) and the non-display periods Td1-Td (m-1). Moreover, the pixel of all Rhine displays in the display periods Tr1-Tr (m-1).
[0131] Next, the actuation which is the pixel after the write-in period Tam when the bit [m-th] digital video signal is inputted into a pixel was started is explained. In addition, in this invention, m can choose the value from 1 to n as arbitration.
[0132] If it writes in in the pixel of the 1st line and Period Tam is started, the bit [m-th] digital video signal will be inputted into the pixel of the 1st line. And after it writes in in the pixel of the 1st line and Period Tam expires, also in the pixel after the 2nd line, it writes in in order and Period Tam is started.
[0133] On the other hand, after it writes in in the pixel of the 1st line and Period Tam expires, a concurrency is carried out to writing in in the pixel of Rhine after the 2nd line, and Period Tam being started, and the display period Trm is started in the pixel of the 1st line. Also in the display period Trm, a pixel displays with the bit [m-th] digital video signal like the display period Trm.
[0134] And after the display period Trm is started in the pixel of the 1st line, also in the pixel after the 2nd line, it writes in in order, Period Tam expires, and the display period Trm is started.
[0135] Next, after the display period Trm is started in the pixel of all Rhine, the display period Trm expires in the pixel of the 1st line, and the write-in period Ta (m+1) is started.
[0136] If it writes in in the pixel of the 1st line and Period Ta (m+1) is started, the bit [m+1st] digital video signal will be inputted into the pixel of the 1st line.
[0137] And in the pixel of the 1st line, the write-in period Ta (m+1) expires. After it writes in in the pixel of the 1st line and Period Ta (m+1) expires, also in the pixel after the 2nd line, the display period Trm expires in order, and the write-in period Ta (m+1) is started.

[0138] In the last pixel of the y-th line, actuation mentioned above is repeatedly performed until the display period Trn corresponding to the bit [n-th] digital video signal expires, and the write-in period Ta and the display period Tr appear repeatedly for every pixel of each Rhine.
[0139] Signs that the gate signal lines Ga1-Gay for writing and the gate signal lines Gb1-Gby for a display are chosen as drawing 7 in the write-in period Tam and the display period Trm are shown.
[0140] For example, if the pixel of the 1st (First Line) line is observed, a pixel will not display in the write-in period Tam. And it is displaying only in the display period Trm. In addition, in drawing 7 , in order to write in and to explain actuation of the pixel in period Tam-Tan and display period Trm-Trn, actuation of the pixel in the write-in period Tam and the display period Trm is illustrated. Therefore, no pixel of Rhine displays in write-in period Tam-Tan. Moreover, the pixel of all Rhine displays in display period Trm-Trn.
[0141] The timing to which the write-in period and display period in m=n -2, and a non-display period appear in drawing 9 in the drive approach of this invention is shown. The axis of abscissa shows time amount and the axis of ordinate shows the location of the gate signal line for writing which a pixel has, and the gate signal line for a display. However, since a write-in period is short, in order to make drawing legible, the arrow head showed the timing by which the write-in periods Ta1-Tan corresponding to each bit are started. Moreover, an arrow head shows a period (sigmaTa1 - sigmaTan) after the write-in period of the pixel of the 1st line is started for every bit until the write-in period of the pixel of the y-th line expires.
[0142] After Trn is completed in the pixel of the 1st line, an one-frame period expires and the write-in period Ta 1 of the next frame period is again started in the pixel of the 1st line. And the actuation mentioned above is repeated again. The timing which an one-frame period starts, and the timing to end have time difference for every pixel of each Rhine.
[0143] One image can be displayed that an one-frame period expires in the pixel of all Rhine.
[0144] As for luminescence equipment, it is desirable to establish 60 or more frame periods in 1 second. When the number of the images displayed in 1 second becomes less than 60, a flicker of an image may begin to be visually conspicuous.
[0145] Moreover, the sum of the die length of all write-in periods is [in / at this invention / the pixel of each Rhine] shorter than an one-frame period. in addition -- and the die length of a display period -- Tr1:Tr2:Tr3:-- it is referred to as :Tr(n-1):Trn=20:21:22:--:2(n-2):2 (n-1). A desired gradation display can be performed among 2n gradation in the combination of this display period.
[0146] By asking for total of the die length of the display period to which the EL element emitted light during the one-frame period, the gradation which the pixel in the frame period concerned displayed is decided. For example, if brightness when a pixel emits light in all display periods is made into 100% at the time of n= 8, when a pixel emits light in Tr1 and Tr2, 1% of brightness can be expressed, and when Tr3, and Tr5 and Tr8 are chosen, 60% of brightness can be expressed.
[0147] The die length of the display period Trm has a ******** more important than a period (sigmaTam) after the write-in period Tam of the pixel of the 1st line is started until the write-in period Tam of the pixel of the y-th line expires.
[0148] Moreover, the display periods Tr1-Trn may be made to appear in what kind of sequence. For example, it is [be / it / under / one frame period / setting] possible to also make a display period appear in the degree of Tr1 in the sequence Tr3, Tr5, Tr2, and --. However, it is required to make it the write-in period in the pixel of each Rhine not lap mutually.
[0149] In addition, it is also possible to omit a capacitor, although it is considering as the structure of forming a capacitor, with the gestalt of this operation in order to hold the electrical potential difference concerning the gate electrode of TFT for EL drive. When TFT for EL drive has the LDD field prepared so that it might lap with a gate electrode through gate dielectric film, the parasitic capacitance generally called gate capacitance is formed in these overlapping fields. You may use positively as a capacitor for holding the electrical potential difference built over the gate electrode of TFT for EL drive in this gate capacitance.
[0150] Since the capacity value of this gate capacitance changes with the area which the above-mentioned gate electrode and the LDD field overlapped, it is decided by the die length of

the LDD field included to those overlapping fields.
[0151] By the drive approach of the gestalt this operation, the die length of the display period of the pixel of each Rhine can be made shorter than a period after the write-in period Ta of the pixel of the 1st line is started until the write-in period Ta of the pixel of the y-th line expires, and the period which in other words writes the digital video signal for 1 bit in all pixels. Therefore, since the die length of the display period corresponding to a lower bit can be shortened even if the number of bits of a digital video signal increases, it is possible to display a high definition image, without flickering a screen.
[0152] Moreover, the luminescence equipment of this invention can obtain fixed brightness, without being influenced by the temperature change. Moreover, in color display, even when the EL element which has a different EL ingredient for every color is prepared, the brightness of the EL element of each color can prevent changing scatteringly and not obtaining a desired color with temperature.
[0153] In addition, although the gestalten 1 and 2 of operation explained the drive approach which displays using a digital video signal, you may display using the video signal of an analog. When displaying using the video signal of an analog, the value of the current which flows to a source signal line can be controlled by the analog video signal, and gradation can be displayed with the magnitude of this current.
[0154]
[Example] Below, the example of this invention is explained.
[0155] (Example 1) This example explains the sequence that the subframe periods SF1-SFn appear, in the drive approach shown in the gestalt 1 of the operation corresponding to a n-bit digital video signal.
[0156] The timing to which n write-in periods (Ta1-Tan) and n display periods (Td1-Tdn) appear in drawing 10 in an one-frame period is shown. The axis of abscissa shows time amount and the axis of ordinate shows the location of the gate signal line for writing which a pixel has, and the gate signal line for a display. Since what is necessary is just to refer to the gestalt 1 of operation about the method of a detailed drive of each pixel, it omits here.
[0157] By the drive approach of this example, the subframe period (this example SFn) which has a display period long No. 1 in an one-frame period is not prepared in the beginning of an one-frame period, and the last. In other words, it is made a configuration in which other subframe periods included at the frame period same before or after the subframe period which has a display period long No. 1 in an one-frame period appear.
[0158] By the above-mentioned configuration, when middle gradation is displayed, it is not recognized by human being's eyes but the display unevenness which had occurred when the display period which emits light in adjacent frame periods adjoined can be ****(ed).
[0159] In addition, in the case of n>=3, the configuration of this example is effective.
[0160] (Example 2) This example explains the drive approach which used the 6-bit digital video signal and which was shown in the gestalt 1 of operation.
[0161] The timing to which n write-in periods (Ta1-Tan) and n display periods (Td1-Tdn) appear in drawing 11 in an one-frame period is shown. The axis of abscissa shows time amount and the axis of ordinate shows the location of the gate signal line for writing which a pixel has, and the gate signal line for a display. Since what is necessary is just to refer to the gestalt 1 of operation about the method of a detailed drive of each pixel, it omits here.
[0162] When [which used the 6-bit digital video signal] driving, at least six subframe periods SF1-SF6 are established within an one-frame period.
[0163] The subframe periods SF1-SF6 support each bit of a 6-bit digital video signal. And the subframe periods SF1-SF6 have six write-in periods (Ta1-Ta6) and n display periods (Td1-Td6).
[0164] The subframe period which has the write-in period Tam corresponding to m (m is number of arbitration of 1-6) bit eye and the display period Tdm serves as SFm. Tdm appears at the degree of the write-in period Tam in the display period corresponding to the same number of bits, and this case.
[0165] It is possible to display one image because write in during an one-frame period and Period Ta and the display period Td appear repeatedly.

[0166] The die length of the display periods Td1-Td6 is Td1:Td2. : -- It is :Td6=20:21. : -- :25 are filled.
[0167] Gradation is expressed as the drive approach of this example by controlling the sum of the die length of the display period in an one-frame period which emits light.
[0168] In addition, it combines with an example 1 freely and the configuration of this example can be carried out.
[0169] (Example 3) This example explains an example of the drive approach which is different in the gestalt 1 of operation which used the n-bit digital video signal.
[0170] The timing to which n+1 write-in period (Ta1-Ta (n+1)) and n display periods (Td1-Td (n+1)) appear in drawing 12 in an one-frame period is shown. The axis of abscissa shows time amount and the axis of ordinate shows the location of the gate signal line for writing which a pixel has, and the gate signal line for a display. Since what is necessary is just to refer to the gestalt of operation about the method of a detailed drive of each pixel, it omits here.
[0171] In this example, subframe period SF1-SFn+1 of n+1 is prepared within an one-frame period corresponding to a n-bit digital video signal. And subframe period SF1-SFn+1 has n+1 write-in period (Ta1-Ta (n+1)) and n display periods (Td1-Td (n+1)).
[0172] The subframe period which has the write-in period Tam (m is the number of the arbitration of one to n+1) and the display period Tdm serves as SFm. Tdm appears at the degree of the write-in period Tam in the display period corresponding to the same number of bits, and this case.
[0173] Subframe period SF1-SFn-1 supports each bit of the digital video signal of 1 - (n-1) a bit. The subframe periods SFn and SF (n+1) support the bit [n-th] digital video signal.
[0174] Moreover, in this example, the subframe periods SFn and SF (n+1) corresponding to the digital video signal of the same bit do not appear continuously. In other words, other subframe periods are established among the subframe periods SFn and SF (n+1) corresponding to the digital video signal of the same bit.
[0175] It is possible to display one image because write in during an one-frame period and Period Ta and the display period Td appear repeatedly.
[0176] The die length of display period Td1-Tdn+1 is Td1:Td2. : -- It is :(Tdn+Td (n+1)) =20:21. : -- :2n-1 is filled.
[0177] Gradation is expressed as the drive approach of this invention by controlling the sum of the die length of the display period in an one-frame period which emits light.
[0178] By the above-mentioned configuration, when middle gradation is displayed, this example is not recognized by human being's eyes compared with the case of examples 1 and 2, but can **** the display unevenness which had occurred when the display period which emits light in adjacent frame periods adjoined.
[0179] In addition, although this example explained the case where there were two subframe periods corresponding to the same bit, this invention is not limited to this. Three or more subframe periods corresponding to the bit same within an one-frame period may be established.
[0180] Moreover, although two or more subframe periods corresponding to the digital video signal of the most significant bit were established in this example, this invention is not limited to this. Two or more subframe periods corresponding to the digital video signal of bits other than the most significant bit may be established. Moreover, the bit in which two or more corresponding subframe periods were prepared is not restricted only to one, but may be made a configuration in which two or more subframe periods correspond to each of some bits.
[0181] In addition, in the case of n>=2, the configuration of this example is effective. Moreover, it combines with examples 1 and 2 freely, and this example can be carried out.
[0182] (Example 4) This example explains the case where 26 gradation is displayed using a 6-bit digital video signal, in the drive approach of the gestalt 2 operation. However, this example explains the case of m= 5. In addition, in this example, an example of the drive approach of this invention is explained and this invention is limited to the configuration of this example neither about the number of bits of a corresponding digital video signal, nor the value of m.
[0183] The timing to which a write-in period, a display period, and a non-display period appear in drawing 13 in the drive approach of this example is shown. The axis of abscissa shows time

amount and the axis of ordinate shows the location of the gate signal line for writing which a pixel has, and the gate signal line for a display. However, since a write-in period is short, in order to make drawing legible, the arrow head showed the timing by which the write-in periods Ta1-Ta6 corresponding to each bit are started. Moreover, an arrow head shows a period (sigmaTa1 - sigmaTa6) after the write-in period of the pixel of the 1st line is started for every corresponding bit until the write-in period of the pixel of the y-th line expires.
[0184] Moreover, since it is the same as the case of the gestalt 1 of operation about detailed actuation of a pixel, explanation is omitted here.
[0185] In the pixel of the 1st line, the write-in period Ta 1 is started first. Initiation of the write-in period Ta 1 inputs the bit [1st] digital video signal into the pixel of the 1st line, as the gestalt of operation showed.
[0186] And after it writes in in the pixel of the 1st line and a period Ta 1 expires, next, also in the pixel after the 2nd line, it writes in in order and a period Ta 1 is started. And the bit [1st] digital video signal is inputted into the pixel of each Rhine like the case of the pixel of the 1st line.
[0187] A concurrency is carried out to writing in in the pixel after the 2nd line and on the other hand, a period Ta 1 being started, and the display period Tr1 is started in the pixel of the 1st line. ** [initiation of the display period Tr1 / display / with the bit / 1st / digital video signal / the pixel of the 1st line]
[0188] And after the display period Tr1 is started in the pixel of the 1st line, also in the pixel after the 2nd line, it writes in in order, a period Ta 1 expires, and the display period Tr1 is started. And the pixel of each Rhine displays with the bit [1st] digital video signal.
[0189] On the other hand, a concurrency is carried out to the display period Tr1 being started in the pixel of Rhine after the 2nd line, the display period Tr1 expires in the pixel of the 1st line, and the non-display period Td1 is started.
[0190] ** [initiation of the non-display period Td1 / stop / the pixel of the 1st line / displaying]

[0191] Next, after the non-display period Td1 is started in the pixel of the 1st line, also in the pixel after the 2nd line, the display period Tr1 expires in order, and the non-display period Td1 is started. The pixel of each Rhine stops therefore, displaying.
[0192] On the other hand, after the non-display period Td1 is started in that the non-display period Td1 is started in the pixel of Rhine after the 2nd line, a concurrency, or all pixels, it writes in in the pixel of the 1st line and a period Ta 2 is started.
[0193] Initiation of the write-in period Ta 2 inputs the bit [2nd] digital video signal into the pixel of the 1st line.
[0194] Before the bit [5th] digital video signal is inputted into a pixel, as for the actuation mentioned above, the write-in period Ta, the display period Tr, and the non-display period Td appear repeatedly for every line crack and pixel of each Rhine.
[0195] Next, the actuation which is the pixel after the write-in period Ta 5 when the bit [5th] digital video signal is inputted into a pixel was started is explained.
[0196] If it writes in in the pixel of the 1st line and a period Ta 5 is started, the bit [5th] digital video signal will be inputted into the pixel of the 1st line. And after it writes in in the pixel of the 1st line and a period Ta 5 expires, also in the pixel after the 2nd line, it writes in in order and a period Ta 5 is started.
[0197] On the other hand, after it writes in in the pixel of the 1st line and a period Ta 5 expires, a concurrency is carried out to writing in in the pixel of Rhine after the 2nd line, and a period Ta 5 being started, and the display period Tr5 is started in the pixel of the 1st line. Also in the display period Tr5, a pixel displays with the bit [5th] digital video signal like the display period Tr5.
[0198] And after the display period Tr5 is started in the pixel of the 1st line, also in the pixel after the 2nd line, it writes in in order, a period Ta 5 expires, and the display period Tr5 is started.
[0199] Next, after the display period Tr5 is started in the pixel of all Rhine, the display period Tr5 expires in the pixel of the 1st line, and the write-in period Ta 6 is started.

[0200] If it writes in in the pixel of the 1st line and a period Ta 6 is started, the bit [6th] digital video signal will be inputted into the pixel of the 1st line.
[0201] And the write-in period Ta 6 expires in the pixel of the 1st line. After it writes in in the pixel of the 1st line and a period Ta 6 expires, also in the pixel after the 2nd line, the display period Tr5 expires in order, and the write-in period Ta 6 is started.
[0202] A concurrency is carried out to writing in in the pixel after the 2nd line and on the other hand, a period Ta 6 being started, and the display period Tr6 is started in the pixel of the 1st line. ** [initiation of the display period Tr6 / display / with the bit / 6th / digital video signal / the pixel of the 1st line]
[0203] And after the display period Tr6 is started in the pixel of the 1st line, also in the pixel after the 2nd line, it writes in in order, a period Ta 6 expires, and the display period Tr6 is started. And the pixel of each Rhine displays with the bit [6th] digital video signal.
[0204] After Tr6 is completed in the pixel of the 1st line, an one-frame period expires in the pixel of the 1st line, and the write-in period Ta 1 of the next frame period is started again. Moreover, after Tr6 is completed in the pixel of the 1st line and Tr6 is completed also in the pixel after the 2nd line, an one-frame period expires in the pixel of each Rhine eye, and the write-in period Ta 1 of the next frame period is started again.
[0205] And the actuation mentioned above is repeated again. The timing which an one-frame period starts, and the timing to end have time difference for every pixel of each Rhine.
[0206] One image can be displayed that an one-frame period expires in the pixel of all Rhine.
[0207] At this example, it is Tr1:Tr2 about the die length of a display period. : -- :Tr5:Tr6=20:21 : — It is referred to as :24:25. A desired gradation display can be performed among 26 gradation in the combination of this display period.
[0208] By asking for total of the die length of the display period to which the EL element emitted light during the one-frame period, the gradation which the pixel in the frame period concerned displayed is decided. For example, in the case of this example, if brightness when a pixel emits light in all display periods is made into 100%, when a pixel emits light in Tr1 and Tr2, 5% of brightness can be expressed, and when Tr3 and Tr5 are chosen, 32% of brightness can be expressed.
[0209] In addition, in this invention, since the write-in period of the pixel of each Rhine does not lap mutually, after the write-in period in the pixel of the y-th line expires, the write-in period in the pixel of the 1st line is started.
[0210] Moreover, in this example, the die length of the display period Tr5 of the pixel of each Rhine has a ******** more important than a period (sigmaTa5) after the write-in period Ta 5 of the pixel of the 1st line is started until the write-in period Ta 5 of the pixel of the y-th line expires.
[0211] Moreover, the display periods Tr1-Tr6 may be made to appear in what kind of sequence. For example, it is [be / it / under / one frame period / setting] possible to also make a display period appear in the degree of Tr1 in the sequence Tr3, Tr5, Tr2, and --. However, it is required to make it the write-in period in the pixel of each Rhine not lap mutually.
[0212] By the drive approach of this invention, the die length of the display period of the pixel of each Rhine can be made shorter than a period after the write-in period Ta of the pixel of the 1st line is started until the write-in period Ta of the pixel of the y-th line expires, and the period which in other words writes the digital video signal for 1 bit in all pixels. Therefore, since the die length of the display period corresponding to a lower bit can be shortened even if the number of bits of a digital video signal increases, it is possible to display a high definition image, without flickering a screen.
[0213] Moreover, the luminescence equipment of this invention can obtain fixed brightness, without being influenced by the temperature change. Moreover, in color display, even when the EL element which has a different EL ingredient for every color is prepared, the brightness of the EL element of each color can prevent changing scatteringly and not obtaining a desired color with temperature.
(Example 5) This example explains the sequence that the display periods Tr1-Tr6 appear, in the drive approach of the gestalt 2 the operation corresponding to a 6-bit digital video signal.

However, this example explains the case of m= 5. In addition, in this example, an example of the drive approach of the gestalt 2 of operation of this invention is explained, and this invention is limited to the configuration of this example neither about the number of bits of a corresponding digital video signal, nor the value of m. In addition, the configuration of this example is effective when the number of bits of a digital video signal is three or more.
[0214] The timing to which a write-in period, a display period, and a non-display period appear in drawing 14 in the drive approach of this example is shown. The axis of abscissa shows time amount and the axis of ordinate shows the location of the gate signal line for writing which a pixel has, and the gate signal line for a display. However, since a write-in period is short, in order to make drawing legible, the arrow head showed the timing by which the write-in periods Ta1-Ta6 corresponding to each bit are started. Moreover, an arrow head shows a period (sigmaTa1 - sigmaTa6) after the write-in period of the pixel of the 1st line is started for every corresponding bit until the write-in period of the pixel of the y-th line expires.
[0215] Moreover, since it is the same as the case of the gestalt 2 of operation about detailed actuation of a pixel, explanation is omitted here.
[0216] In the pixel of the 1st line, the write-in period Ta 4 is started first. Initiation of the write-in period Ta 4 inputs the bit [4th] digital video signal into the pixel of the 1st line.
[0217] And after it writes in in the pixel of the 1st line and a period Ta 4 expires, next, also in the pixel after the 2nd line, it writes in in order and a period Ta 4 is started. And the bit [4th] digital video signal is inputted into the pixel of each Rhine like the case of the pixel of the 1st line.
[0218] A concurrency is carried out to writing in in the pixel after the 2nd line and on the other hand, a period Ta 4 being started, and the display period Tr4 is started in the pixel of the 1st line. ** [initiation of the display period Tr4 / display / with the bit / 4th / digital video signal / the pixel of the 1st line]
[0219] And after the display period Tr4 is started in the pixel of the 1st line, also in the pixel after the 2nd line, it writes in in order, a period Ta 4 expires, and the display period Tr4 is started. And the pixel of each Rhine displays with the bit [4th] digital video signal.
[0220] On the other hand, after the display period Tr4 begins in the pixel of Rhine after the 2nd line, the display period Tr4 expires in the pixel of the 1st line, and the non-display period Td4 is started. In addition, a concurrency is carried out to the display period Tr4 being started in the pixel of Rhine after the 2nd line, the display period Tr4 expires in the pixel of the 1st line, and the non-display period Td4 may be started.
[0221] ** [initiation of the non-display period Td4 / stop / the pixel of the 1st line / displaying]

[0222] Next, after the non-display period Td4 is started in the pixel of the 1st line, also in the pixel after the 2nd line, the display period Tr4 expires in order, and the non-display period Td4 is started. The pixel of each Rhine stops therefore, displaying.
[0223] On the other hand, after the non-display period Td4 is started in that the non-display period Td4 is started in the pixel of Rhine after the 2nd line, a concurrency, or all pixels, it writes in in the pixel of the 1st line and a period Ta 5 is started.
[0224] If it writes in in the pixel of the 1st line and a period Ta 5 is started, the bit [5th] digital video signal will be inputted into the pixel of the 1st line. And after it writes in in the pixel of the 1st line and a period Ta 5 expires, also in the pixel after the 2nd line, it writes in in order and a period Ta 5 is started.
[0225] On the other hand, after it writes in in the pixel of the 1st line and a period Ta 5 expires, a concurrency is carried out to writing in in the pixel of Rhine after the 2nd line, and a period Ta 5 being started, and the display period Tr5 is started in the pixel of the 1st line. Also in the display period Tr5, a pixel displays with the bit [5th] digital video signal like the display period Tr5.
[0226] And after the display period Tr5 is started in the pixel of the 1st line, also in the pixel after the 2nd line, it writes in in order, a period Ta 5 expires, and the display period Tr5 is started.
[0227] Next, after the display period Tr5 is started in the pixel of all Rhine, the display period Tr5

expires in the pixel of the 1st line, and the write-in period Ta 2 is started.
[0228] If it writes in in the pixel of the 1st line and a period Ta 2 is started, the bit [2nd] digital video signal will be inputted into the pixel of the 1st line.
[0229] And after it writes in in the pixel of the 1st line and a period Ta 2 expires, next, also in the pixel after the 2nd line, it writes in in order and a period Ta 2 is started. And the bit [2nd] digital video signal is inputted into the pixel of each Rhine like the case of the pixel of the 1st line.
[0230] A concurrency is carried out to writing in in the pixel after the 2nd line and on the other hand, a period Ta 2 being started, and the display period Tr2 is started in the pixel of the 1st line. ** [initiation of the display period Tr2 / display / with the bit / 2nd / digital video signal / the pixel of the 1st line]
[0231] And after the display period Tr2 is started in the pixel of the 1st line, also in the pixel after the 2nd line, it writes in in order, a period Ta 2 expires, and the display period Tr2 is started. And the pixel of each Rhine displays with the bit [2nd] digital video signal.
[0232] On the other hand, a concurrency is carried out to the display period Tr2 being started in the pixel of Rhine after the 2nd line, the display period Tr2 expires in the pixel of the 1st line, and the non-display period Td2 is started.
[0233] ** [initiation of the non-display period Td2 / stop / the pixel of the 1st line / displaying]

[0234] Next, after the non-display period Td2 is started in the pixel of the 1st line, also in the pixel after the 2nd line, the display period Tr2 expires in order, and the non-display period Td2 is started. The pixel of each Rhine stops therefore, displaying.
[0235] On the other hand, after the non-display period Td2 is started in that the non-display period Td2 is started in the pixel of Rhine after the 2nd line, a concurrency, or all pixels, it writes in in the pixel of the 1st line and a period Ta 3 is started.
[0236] Before the digital video signal of all the bits of 1-6 is inputted into a pixel, as for the actuation mentioned above, the write-in period Ta, the display period Tr, and the non-display period Td appear repeatedly for every line crack and pixel of each Rhine.
[0237] After all the display periods Tr1-Tr6 expire in the pixel of the 1st line, an one-frame period expires in the pixel of the 1st line, and the write-in period (this example Ta4) of the beginning of the next frame period is started again. Moreover, after an one-frame period expires in the pixel of the 1st line, an one-frame period expires also in the pixel after the 2nd line, and the write-in period Ta 4 of the next frame period is started again.
[0238] And the actuation mentioned above is repeated again. The timing which an one-frame period starts, and the timing to end have time difference for every pixel of each Rhine.
[0239] One image can be displayed that an one-frame period expires in the pixel of all Rhine.
[0240] At this example, it is Tr1:Tr2 about the die length of a display period. : -- :Tr5:Tr6=20:21 : -- It is referred to as :24:25. A desired gradation display can be performed among 26 gradation in the combination of this display period.
[0241] By asking for total of the die length of the display period to which the EL element emitted light during the one-frame period, the gradation which the pixel in the frame period concerned displayed is decided. For example, in the case of this example, if brightness when a pixel emits light in all display periods is made into 100%, when a pixel emits light in Tr1 and Tr2, 5% of brightness can be expressed, and when Tr3 and Tr5 are chosen, 32% of brightness can be expressed.
[0242] In addition, in this invention, since the write-in period of the pixel of each Rhine does not lap mutually, after the write-in period in the pixel of the y-th line expires, the write-in period in the pixel of the 1st line is started.
[0243] Moreover, in this example, the die length of the display period Tr5 of the pixel of each Rhine has a ******** more important than a period (sigmaTa5) after the write-in period Ta 5 of the pixel of the 1st line is started until the write-in period Ta 5 of the pixel of the y-th line expires.
[0244] Moreover, the display periods Tr1-Tr6 may be made to appear in what kind of sequence. For example, it is [be / it / under / one frame period / setting] possible to also make a display

period appear in the degree of Tr1 in the sequence Tr3, Tr5, Tr2, and --. However, it is required to make it the write-in period in the pixel of each Rhine not lap mutually.
[0245] By the drive approach of this example, the die length of the display period of the pixel of each Rhine can be made shorter than a period after the write-in period Ta of the pixel of the 1st line is started until the write-in period Ta of the pixel of the y-th line expires, and the period which in other words writes the digital video signal for 1 bit in all pixels. Therefore, since the die length of the display period corresponding to a lower bit can be shortened even if the number of bits of a digital video signal increases, it is possible to display a high definition image, without flickering a screen.
[0246] Moreover, the luminescence equipment of this invention can obtain fixed brightness, without being influenced by the temperature change. Moreover, in color display, even when the EL element which has a different EL ingredient for every color is prepared, the brightness of the EL element of each color can prevent changing scatteringly and not obtaining a desired color with temperature.
[0247] In addition, by the drive approach of this example, a display period (this example Tr6) long No. 1 is not prepared in the beginning of an one-frame period, and the last in an one-frame period. In other words, it is made a configuration in which other display periods included in an one-frame period at the frame period same before or after a display period long No. 1 appear.
[0248] By the above-mentioned configuration, when middle gradation is displayed, it is not recognized by human being's eyes but the display unevenness which had occurred when the display period which emits light in adjacent frame periods adjoined can be ****(ed).
[0249] It combines with an example 4 freely and this example can be carried out.
[0250] (Example 6) This example explains an example of the drive approach which is different in the gestalt 2 of operation which used the n-bit digital video signal. However, this example explains the case of m=n -2.
[0251] the display period Trn corresponding to the digital video signal of the most significant bit by the drive approach of this example -- the 1st -- display period Trn_1 and the 2nd -- it is dividing into display period Trn_2. and the 1st -- display period Trn_1 and the 2nd -- display period Trn_2 -- respectively -- alike -- corresponding -- the 1st -- write-in period Tan_1 and the 2nd -- write-in period Tan_2 are prepared.
[0252] The timing to which a write-in period, a display period, and a non-display period appear in drawing 15 in the drive approach of this example is shown. The axis of abscissa shows time amount and the axis of ordinate shows the location of the gate signal line for writing which a pixel has, and the gate signal line for a display. However, since a write-in period is short, in order to make drawing legible, the arrow head showed the timing by which the write-in periods Ta1-Ta (n-1) corresponding to each bit, Tan_1, and Tan_2 are started. Moreover, an arrow head shows a period (sigmaTa1 - sigmaTa (n-1), sigmaTan_1, sigmaTan_2) after the write-in period of the pixel of the 1st line is started for every corresponding bit until the write-in period of the pixel of the y-th line expires.
[0253] Moreover, since it is the same as the case of the gestalt 2 of operation about detailed actuation of a pixel, explanation is omitted here.
[0254] moreover, the 1st corresponding to the digital video signal of the bit same in this example -- display period Trn_1 and the 2nd -- the display period corresponding to other bits is established among display period Trn_2.
[0255] The die length of the display periods Tr1-Trn, Trn_1, and Trn_2 is Tr1:Tr2. : -- It is :Tr(n-1):(Trn_1+Trn_2) =20:21. : -- :2n-1 is filled.
[0256] Gradation is expressed as the drive approach of this invention by controlling the sum of the die length of the display period in an one-frame period which emits light.
[0257] By the above-mentioned configuration, when middle gradation is displayed, this example is not recognized by human being's eyes compared with the case of examples 4 and 5, but can **** the display unevenness which had occurred when the display period which emits light in adjacent frame periods adjoined.
[0258] In addition, although this example explained the case where there were two display periods corresponding to the same bit, this invention is not limited to this. Three or more display

periods corresponding to the bit same within an one-frame period may be established.
[0259] Moreover, although two or more display periods corresponding to the digital video signal of the most significant bit were established in this example, this invention is not limited to this. Two or more display periods corresponding to the digital video signal of bits other than the most significant bit may be established. Moreover, the bit in which two or more corresponding display periods were prepared is not restricted only to one, but may be made a configuration in which two or more display periods correspond to each of some bits.
[0260] In addition, in the case of n>=2, the configuration of this example is effective. Moreover, it combines with examples 4 or 5 freely, and this example can be carried out.
[0261] (Example 7) This example explains the configuration of the drive circuit (a source signal-line drive circuit and gate signal line drive circuit) which the luminescence equipment of this invention has.
[0262] A block diagram shows the configuration of the source signal-line drive circuit 601 to drawing 16 . For 602, as for a store circuit A and 604, a shift register and 603 are [a store circuit B and 605] current regulator circuits.
[0263] The clock signal CLK and the start pulse signal SP are inputted into the shift register 602. Moreover, the digital video signal (Digital Video Signals) is inputted into the store circuit A602, and the latch signal (Latch Signals) is inputted into the store circuit B603. The fixed current Ic outputted from a current regulator circuit 604 is inputted into a source signal line.
[0264] The more detailed configuration of the source signal-line drive circuit 601 is shown in drawing 17 .
[0265] A timing signal is generated by inputting a clock signal CLK and the start pulse signal SP into a shift register 602 from predetermined wiring. A timing signal is inputted into two or more latches A (LATA_1 - LATA_x) whom a store circuit A603 has, respectively. In addition, the timing signal generated in the shift register 602 at this time may be made a configuration which inputs into two or more latches A (LATA_1 - LATA_x) whom a store circuit A603 has, respectively after carrying out buffer magnification with a buffer etc.
[0266] If a timing signal is inputted into a store circuit A603, synchronizing with this timing signal, the digital video signal for 1 bit inputted into the video signal line 610 will be written in and held at each of two or more latches A (LATA_1-LATA_x) at order.
[0267] In addition, although the digital video signal is inputted into two or more latches A (LATA_1 - LATA_x) whom a store circuit A603 has in order in this example in case a digital video signal is incorporated to a store circuit A603, this invention is not limited to this configuration. The latch of two or more stages which a store circuit A603 has may be divided into some groups, and the so-called division drive which inputs a digital video signal into coincidence in parallel for every group may be performed. In addition, the number of the groups at this time is called the number of partitions. For example, when a latch is divided into a group every four stages, it is said that a division drive is carried out by quadrisection.
[0268] Time amount until the writing of a digital video signal is briefly completed to the latch of all the stages of a store circuit A603 is called the Rhine period. In fact, the period when the horizontal blanking interval was added to the above-mentioned Rhine period may be included at the Rhine period.
[0269] Termination of an one-line period supplies a latch signal (Latch Signal) to two or more latches B (LATB_1 - LATB_x) whom a store circuit B604 has through the latch signal line 609. At this moment, the digital video signals currently held at two or more latches A (LATA_1-LATA_x) whom a store circuit A603 has are written in two or more latches B (LATB_1 - LATB_x) whom a store circuit B604 has all at once, and are held.
[0270] Based on the timing signal from a shift register 602, the writing of the following digital video signal for 1 bit is performed in the store circuit A603 which finished sending out a digital video signal to a store circuit B604 one by one.
[0271] During the one-line period of eye this 2 order, it is written in a store circuit B604, and the digital video signal currently held is inputted into a current regulator circuit 605.
[0272] The current regulator circuit 605 has two or more current setting circuits (C1-Cx). If a digital video signal is inputted into each of a current setting circuit (C1-Cx), using the

information on 1 or 0 which this digital video signal has, the fixed current Ic will flow to a source signal line, the potential of the current supply lines V1-Vx will be given to a source signal line, or either will be chosen.
[0273] An example of the concrete configuration of the current setting circuit C1 is shown in drawing 18 . In addition, it has the configuration same as the current setting circuits C2-Cx.
[0274] The current setting circuit C1 has a constant current source 631, four transmission gates SW1-SW4, and two inverters Inb1 and Inb2.
[0275] Switching of SW1-SW4 is controlled by the digital video signal outputted from LATB_1 which a store circuit B604 has. In addition, the digital video signal inputted into SW1 and SW3 and the digital video signal inputted into SW2 and SW4 are reversed by Inb1 and Inb2. Therefore, when SW1 and SW3 are ON, and OFF, and SW1 and SW3 are OFF as for SW2 and SW4, SW2 and SW4 are ON.
[0276] When SW1 and SW3 are ON, Current Ic is inputted into the source signal line S1 through SW1 and SW3 from a constant current source 631.
[0277] Conversely, when SW2 and SW4 are ON, the current Ic from a constant current source 631 is dropped on a ground through SW2. Moreover, the power-source potential of the current supply lines V1-Vx is given to the source signal line S1 through SW4.
[0278] With reference to drawing 17 , the aforementioned actuation is again performed to coincidence in all the current setting circuits (C1-Cx) that a current regulator circuit 605 has within an one-line period. Therefore, it is chosen whether in all source signal lines, the fixed current Ic is passed by the digital video signal or power-source potential is given.
[0279] In addition, another circuits, such as a decoder circuit, are used instead of a shift register, and you may make it write a digital video signal in a latch circuit in order.
[0280] Next, the configuration of the gate signal line drive circuit for writing and the gate signal line drive circuit for a display is explained. However, since the configuration of the gate signal line drive circuit for writing and the gate signal line drive circuit for a display is almost the same, it represents here and only the gate signal line drive circuit for writing is explained.
[0281] Drawing 19 is the block diagram showing the configuration of the gate signal line drive circuit 641 for writing.
[0282] The gate signal line drive circuit 641 for writing has the shift register 642 and the buffer 643, respectively. Moreover, depending on the case, you may have the level shifter.
[0283] In the gate signal line drive circuit 641 for writing, a timing signal is generated by inputting Clock CLK and the start pulse signal SP into a shift register 642. Buffer magnification is carried out in a buffer 643, and the generated timing signal is supplied to the selected gate signal line for writing.
[0284] The gate electrode of TFT for the 1st switching of the pixel for one line and TFT for the 2nd switching is connected to the gate signal line for writing. And since TFT(s) for the 1st switching and TFT(s) for the 2nd switching of a pixel for one line must be turned ON all at once, what has that possible a buffer 643 passes a big current is used.
[0285] In addition, in the case of the gate signal line drive circuit for a display, TFT(s) for EL drive connected to all the gate signal lines for a display are turned ON all at once in each display period. Therefore, the wave differs from the clock signal CLK and the start pulse signal SP which are inputted into the shift register of the gate signal line drive circuit for writing.
[0286] In addition, another circuits, such as a decoder circuit, are used instead of a shift register, a gate signal is chosen, and you may make it supply a timing signal.
[0287] The drive circuit used in this invention is not limited to the configuration shown by this example.
[0288] It combines with an example 1 - an example 6 freely, and this example can be carried out.

[0289] (Example 8) This example shows an example of the plan of a pixel which has the configuration shown in drawing 1 .
[0290] The plan of the pixel of this example is shown in drawing 20 . The pixel has the source signal line Si, the current supply line Vi, the gate signal line Gaj for writing, and the gate signal line Gbj for a display. The source signal line Si is taken about with a part and the connection

wiring 182 so that the gate signal line Gj may not be contacted in the part which laps with the gate signal line Gaj for writing, and the gate signal line Gbj for a display.
[0291] 102 and 103 are TFT for the 1st switching, and TFT for the 2nd switching, respectively. Moreover, 104 and 105 are TFT for current control, and TFT for EL drive, respectively.
[0292] One side is connected to the source signal line Si for the source field and drain field of TFT102 for the 1st switching through the connection wiring 190, and another side is connected to the drain field of TFT104 for current control through the connection wiring 183. Moreover, one side is connected to the drain field of TFT104 for current control for the source field and drain field of TFT103 for the 2nd switching through the connection wiring 183, and another side is connected to the connection wiring 184 and the gate wiring 185. In addition, some gate wiring 185 is functioning as a gate electrode of TFT for current control.
[0293] A part of gate signal line Gaj for writing is functioning as a gate electrode of TFT102 for the 1st switching, and TFT103 for the 2nd switching.
[0294] Moreover, some of current supply lines Vi and gate wiring 185 have lapped on both sides of the interlayer insulation film in between, and an overlapping part becomes a capacitor 107.
[0295] The source field of TFT104 for current control is connected to the current supply line Vi, and the drain field is connected to the source field of TFT105 for EL drive through the connection wiring 186. The drain field of TFT105 for EL drive is connected to the pixel electrode 181. Moreover, a part of gate signal line Gbj for a display is functioning as a gate electrode of TFT105 for EL drive.
[0296] In addition, the pixel which the luminescence equipment of this invention has is not limited to the configuration shown in drawing 20 . Moreover, it combines with examples 1-7 freely, and the configuration of this example can be carried out.
[0297] (Example 9) This example explains how to produce TFT of the picture element part of the luminescence equipment of this invention. In addition, TFT which the drive circuit (a source signal-line side drive circuit, the gate signal line side drive circuit for writing, gate signal line side drive circuit for a display) prepared around a picture element part has may be formed on the same substrate as TFT of a picture element part at coincidence.
[0298] First, as shown in drawing 21 (A), the substrate film 5002 which consists of insulator layers, such as an oxidation silicone film, a silicon nitride film, or an oxidation silicon nitride film, is formed on the substrate 5001 which consists of glass, such as barium borosilicate glass represented by #7059 glass of Corning, Inc., #1737 glass, etc., or alumino borosilicate glass. For example, 10-200 [nm] (preferably 50-100 [nm]) formation of SiH4, NH3, and the oxidation silicon nitride film 5002a produced from N2O is carried out by the plasma-CVD method, and laminating formation of the oxidation nitriding hydrogenation silicone film 5002b similarly produced from SiH4 and N2O is carried out at the thickness of 50-200 [nm] (preferably 100-150 [nm]). Although this example showed the substrate film 5002 as two-layer structure, you may form as structure which carried out the laminating the monolayer of said insulator layer, or more than two-layer.
[0299] The island-shape semi-conductor layers 5004-5006 are formed by the crystalline substance semi-conductor film which produced the semi-conductor film which has amorphous structure using the laser crystallizing method or the well-known heat crystallizing method. The thickness of these island-shape semi-conductor layers 5004-5006 is formed by the thickness of 25-80 [nm] (preferably 30-60 [nm]). Although there is no limitation in the ingredient of the crystalline substance semi-conductor film, it is good to form with silicon or a silicon germanium (SiGe) alloy preferably.
[0300] In order to produce the crystalline substance semi-conductor film by the laser crystallizing method, the excimer laser of a pulse oscillation mold or a continuation luminescence mold, and an YAG laser and YVO4 laser are used. When using such laser, it is good to use the approach of condensing to a line the laser light emitted from the laser oscillation machine by optical system, and irradiating the semi-conductor film. Although an operation person makes **** selection, the conditions of crystallization are made into the pulse oscillation frequency 300 [Hz] when using an excimer laser, and set a laser energy consistency to 100-400 [mJ/cm2] (typically 200-300 [mJ/cm2]). Moreover, it is good to consider as the pulse oscillation

frequencies 30-300 [kHz] using the 2nd higher harmonic, in using an YAG laser, and to set a laser energy consistency to 300-600 [mJ/cm2] (typically 350-500 [mJ/cm2]). and width of face 100-1000 [mum], for example, the laser light which condensed to the line by 400 [mum], -- the whole substrate surface -- crossing -- irradiating -- the line at this time -- the rate of superposition of laser light (rate of overlap) is performed as 50-90 [%].

[0301] Subsequently, wrap gate dielectric film 5007 is formed for the island-shape semiconductor layers 5004-5006. Gate dielectric film 5007 is formed using a plasma-CVD method or a spatter by the insulator layer which sets thickness to 40-150 [nm], and contains silicon. At this example, it forms with an oxidation silicon nitride film by the thickness of 120 [nm]. Of course, gate dielectric film is not limited to such an oxidation silicon nitride film, and may use the insulator layer containing other silicon as a monolayer or a laminated structure. For example, when using an oxidation silicone film, TEOS (Tetraethyl Orthosilicate) and O2 can be mixed by the plasma-CVD method, and it can consider as reaction pressure 40 [Pa] and the substrate temperature 300-400 [**], it can be made to be able to discharge by the RF (13.56 [MHz]) and power flux density 0.5-0.8 [W/cm2], and can form. Thus, the oxidation silicone film produced can acquire a property good as gate dielectric film by heat annealing of 400-500 [**] after that.

[0302] And the 1st electric conduction film 5008 for forming a gate electrode on gate dielectric film 5007 and the 2nd electric conduction film 5009 are formed. In this example, the 1st electric conduction film 5008 is formed in the thickness of 50-100 [nm] by Ta, and the 2nd electric conduction film 5009 is formed in the thickness of 100-300 [nm] by W.

[0303] By the spatter, Ta film is formed by carrying out the spatter of the target of Ta by Ar. In this case, if Xe and Kr of optimum dose are added to Ar, the internal stress of Ta film can be eased and exfoliation of the film can be prevented. Moreover, although the resistivity of Ta film of alpha phase is 20 [muomegacm] extent and it can be used for a gate electrode, the resistivity of Ta film of a parent phase is unsuitable for being 180 [muomegacm] extent and considering as a gate electrode. In order to form Ta film of alpha phase, if tantalum nitride with the crystal structure near alpha phase of Ta is formed in the substrate of Ta by the thickness of 10-50 [nm] extent, Ta film of alpha phase can be obtained easily.

[0304] In forming W film, it forms W by the spatter used as the target. In addition, it can also form with the heat CVD method using 6 tungsten fluoride (WF6). Anyway, in order to use it as a gate electrode, it is necessary to attain low resistance-ization, and as for the resistivity of W film, carrying out to below 20 [muomegacm] is desirable. In W, although W film can attain low resistivity-ization by enlarging crystal grain, when there are many impurity elements, such as oxygen, crystallization is checked and forms it into high resistance. From this, when based on a spatter, resistivity 9-20 [muomegacm] can be realized using W target of purity 99.9999 [%] by considering enough and forming W film so that there may be no mixing of the impurity out of a gaseous phase further at the time of membrane formation.

[0305] In addition, in this example, although Ta and the 2nd electric conduction film 5009 were set to W for the 1st electric conduction film 5008, it is not limited especially but the element with which all were chosen from Ta, W, Ti, Mo, aluminum, Cu, etc., or said element may be formed with the alloy ingredient or compound ingredient used as a principal component. Moreover, the semi-conductor film represented by the polycrystal silicone film which doped impurity elements, such as Lynn, may be used. As a desirable thing, with an example of other combination other than this example Form the 1st electric conduction film 5008 by tantalum nitride (TaN), and set the 2nd electric conduction film 5009 to W, and it is combined. The 1st electric conduction film 5008 is formed by tantalum nitride (TaN), it combines, the 1st electric conduction film 5008 is formed by tantalum nitride (TaN), and the combination for which the 2nd electric conduction film 5009 is set to aluminum and which sets the 2nd electric conduction film 5009 to Cu is mentioned. (Drawing 21 (A))

[0306] Next, 1st etching processing for forming the mask 5010 by the resist and forming an electrode and wiring is performed. In this example, it carries out by mixing CF4 and Cl2 in the gas for etching, supplying RF (13.56 [MHz]) power of 500 [W] to the electrode of a coil mold by the pressure of 1 [Pa] using the ICP (Inductively Coupled Plasma: inductive-coupling mold plasma) etching method, and generating the plasma. RF (13.56 [MHz]) power of 100 [W] is supplied also

to a substrate side (sample stage), and a negative auto-bias electrical potential difference is impressed substantially. When CF4 and Cl2 are mixed, W film and Ta film are etched to the same extent.

[0307] On the above-mentioned etching conditions, the edge of the 1st conductive layer and the 2nd conductive layer serves as a taper configuration by having been suitable in the configuration of the mask by the resist according to the effectiveness of the bias voltage impressed to a substrate side. The include angle of the taper section becomes 15-45 degrees. In order to etch without leaving residue on gate dielectric film, it is good to make etching time increase at a rate of 10-20 [%] extent. Since the selection ratios of an oxidization silicon nitride film to W film are 2-4 (typically 3), 20-50 [nm] extent etching of the field which the oxidization silicon nitride film exposed will be carried out by over etching processing. In this way, the conductive layers 5011-5015 (the 1st conductive layers 5011a-5015a and 2nd conductive layer 5011b-5015b) of the 1st configuration which consists of the 1st conductive layer and 2nd conductive layer by 1st etching processing are formed. At this time, the field which 20-50 [nm] extent etching of the field which is not covered by the conductive layers 5011-5015 of the 1st configuration was carried out, and became thin is formed in gate dielectric film 5007.

[0308] And the impurity element which performs 1st doping processing and gives N type is added. What is necessary is just to perform the approach of doping with the ion doping method or ion-implantation. The conditions of the ion doping method set a dose to 1x1013 to 5x1014 [atoms/cm2], and perform acceleration voltage as 60-100 [keV]. the element which belongs to 15 groups as an impurity element which gives N type -- typical -- Lynn -- although (P) or arsenic (As) is used -- here -- Lynn -- (P) is used. In this case, it becomes a mask to the impurity element with which conductive layers 5012-5015 give N type, and the 1st impurity range 5017-5023 is formed in self align. In the 1st impurity range 5017-5023, the impurity element which gives N type by the density range of 1x1020 to 1x1021 [atoms/cm3] is added. (Drawing 21 (B))

[0309] Next, as shown in drawing 21 (C), a resist mask performs 2nd etching processing, not removed. CF4, and Cl2 and O2 are used for etching gas, and W film is etched alternatively. At this time, the conductive layers 5025-5029 (the 1st conductive layers 5025a-5029a and 2nd conductive layer 5025b-5029b) of the 2nd configuration are formed by 2nd etching processing. At this time, the field which 20-50 [nm] extent etching of the field which is not covered by the conductive layers 5025-5029 of the 2nd configuration was carried out at the pan, and became thin is formed in gate dielectric film 5007.

[0310] The etching reaction by the mixed gas of CF4 and Cl2 of W film or Ta film can be guessed from the vapor pressure of the radical or ion kind generated, and a resultant. If the vapor pressure of the fluoride of W and Ta and a chloride is compared, WF6 which is the fluoride of W is extremely high, and WCl5, TaF5, and TaCl5 of others have it. [comparable] Therefore, W film and Ta film are etched in the mixed gas of CF4 and Cl2. However, if O2 of optimum dose is added to this mixed gas, CF4 and O2 will react, it will be set to CO and F, and F radical or F ion will be generated so much. Consequently, the etch rate of W film with the high vapor pressure of a fluoride increases. On the other hand, even if, as for Ta, F increases, there are few increments in an etch rate relatively. Moreover, since Ta tends to oxidize as compared with W, the front face of Ta oxidizes by adding O2. In order that the oxide of Ta may react neither with a fluorine nor chlorine, the etch rate of Ta film falls further. Therefore, it becomes possible to become possible to make a difference to the etch rate of W film and Ta film, and to make the etch rate of W film larger than Ta film.

[0311] And as shown in drawing 22 (A), 2nd doping processing is performed. In this case, the impurity element which lowers a dose and gives N type as conditions for high acceleration voltage rather than the 1st doping processing is doped. For example, a new impurity range is formed inside the 1st impurity range which set acceleration voltage to 70-120 [keV], carried out with the dose of 1x1013 [atoms/cm2], and was formed in the island-shape semi-conductor layer by drawing 21 (B). Doping uses the conductive layers 5026-5029 of the 2nd configuration as a mask to an impurity element, and it dopes them so that an impurity element may be added by the field of the 1st conductive layera [5026]-5029a bottom. In this way, the 3rd impurity range

5032-5035 is formed. The concentration of Lynn (P) added by this 3rd impurity range 5032-5035 has the loose concentration gradient according to the thickness of the taper section of the 1st conductive layer 5026a-5029a. In addition, in the semi-conductor layer which laps with the taper section of the 1st conductive layer 5026a-5029a, although high impurity concentration is low a little toward the edge of the taper section of the 1st conductive layer 5026a-5029a to the inside, it is almost comparable concentration.

[0312] As shown in drawing 22 (B), 3rd etching processing is performed. CHF6 is used for etching gas and it carries out using a reactive-ion-etching method (the RIE method). The field where the taper section of the 1st conductive layer 5025a-5029a is etched partially, and the 1st conductive layer laps with a semi-conductor layer by 3rd etching processing is reduced. By 3rd etching processing, the conductive layers 5036-5040 (the 1st conductive layers 5036a-5040a and 2nd conductive layer 5036b-5040b) of the 3rd configuration are formed. At this time, the field which 20-50 [nm] extent etching of the field which is not covered by the conductive layers 5036-5040 of the 3rd configuration was carried out at the pan, and became thin is formed in gate dielectric film 5007.

[0313] The 2nd impurity range 5032b-5035b between the 3rd impurity range 5032a-5035a which laps with the 1st conductive layer 5037a-5040a in the 3rd impurity range 5032-5035 by 3rd etching processing, and the 1st impurity range and the 3rd impurity range is formed.

[0314] And as shown in drawing 22 (C), the 4th impurity range 5043-5054 of a conductivity type contrary to the 1st conductivity type is formed in the island-shape semi-conductor layers 5005 and 5006 which form the P channel mold TFT. The conductive layers 5039b and 5040b of the 3rd configuration are used as a mask to an impurity element, and an impurity range is formed in self align. At this time, the island-shape semi-conductor layers 5005 and 5005 and the wiring section 5036 which form the N channel mold TFT cover the whole surface with the resist mask 5200. Although Lynn is added by impurity ranges 5043-5054 by concentration different, respectively, it forms by the ion doping method using diboron hexahydride (B-2 H6), and is made for high impurity concentration to be set to 2x1020 to 2x1021 [atoms/cm3] also in which the field.

[0315] An impurity range is formed in each island-shape semi-conductor layer at the process to the above. The conductive layers 5037-5040 of the 3rd configuration which lap with an island-shape semi-conductor layer function as a gate electrode. Moreover, 5036 functions as an island-shape source signal line.

[0316] After removing the resist mask 5200, the process which activates the impurity element added by each island-shape semi-conductor layer for the purpose of control of a conductivity type is performed. This process is performed by the heat annealing method for using a furnace annealing furnace. In addition, the laser annealing method or the rapid thermal annealing method (RTA law) is applicable. By the heat annealing method, preferably, in the nitrogen-gas-atmosphere mind below 0.1 [ppm], it carries out by 500-600 [**] typically, and an oxygen density performs [400-700 [**] and] heat treatment of 4 hours this example below 1 [ppm] 500 [**]. However, when the wiring material used for the conductive layers 5036-5040 of the 3rd configuration is weak with heat, it is desirable to be activated after forming an interlayer insulation film (let silicon be a principal component), in order to protect wiring etc.

[0317] Furthermore, in the ambient atmosphere containing the hydrogen of 3-100 [%], heat treatment of 1 - 12 hours is performed by 300-450 [**], and the process which hydrogenates an island-shape semi-conductor layer is performed. This process is a process which carries out termination of the dangling bond of a semi-conductor layer by the hydrogen excited thermally. As other means of hydrogenation, plasma hydrogenation (the hydrogen excited by the plasma is used) may be performed.

[0318] Subsequently, as shown in drawing 23 (A), the 1st interlayer insulation film 5055 is formed by the thickness of 100-200 [nm] from an oxidation silicon nitride film. After forming a contact hole to the 1st interlayer insulation film 5055, the 2nd interlayer insulation film 5056, and gate dielectric film 5007 after forming the 2nd interlayer insulation film 5056 which consists of an organic insulating material ingredient on it, and carrying out patterning formation of the connection wiring 5057-5062, patterning formation of the pixel electrode 5064 which touches the connection wiring (drain wiring) 5062 is carried out. In addition, source wiring and drain wiring are

included in connection wiring. Source wiring is wiring connected to the source field of a barrier layer, and drain wiring means wiring connected to the drain field.
[0319] As the 2nd interlayer insulation film 5056, polyimide, a polyamide, an acrylic, BCB (benz-cyclo-butene), etc. can be used as the organic resin using the film made from organic resin. Since especially the 2nd interlayer insulation film 5056 has the strong implications of flattening, its acrylic excellent in surface smoothness is desirable. At this example, the acrylic film is formed by the thickness which can fully carry out flattening of the level difference formed of TFT. desirable -- 1-5 [mum] (still more preferably 2-4 [mum]) -- then, it is good.
[0320] Formation of a contact hole forms the contact hole which arrives at the impurity ranges 5017-5019 of N type, or the impurity ranges 5043, 5048, 5049, and 5054 of P type, the contact hole which reaches wiring 5036, the contact hole (not shown) which reaches a current supply line, and the contact hole (not shown) which reaches a gate electrode using dry etching or wet etching, respectively.
[0321] Moreover, what carried out patterning of the cascade screen of the three-tiered structure which carried out the aluminum film which contains 100 [nm] and Ti for Ti film by 300 [nm] as connection wiring 5057-5062, and carried out continuation formation of the Ti film 150 [nm] by the spatter to the desired configuration is used. Of course, other electric conduction film may be used.
[0322] Moreover, in this example, the ITO film was formed in the thickness of 110 [nm] as a pixel electrode 5064, and patterning was performed. Contact is taken by arranging the pixel electrode 5064 so that it may lap in contact with the connection wiring 5062. Moreover, the transparence electric conduction film which mixed the zinc oxide (ZnO) of 2-20 [%] may be used for indium oxide. This pixel electrode 5064 turns into an anode plate of an EL element. (Drawing 23 (A))
[0323] Next, as shown in drawing 23 (B), the insulator layer (this example oxidation silicon film) containing silicon is formed in the thickness of 500 [nm], opening is formed in the location corresponding to the pixel electrode 5064, and the 3rd interlayer insulation film 5065 which functions as a bank is formed. In case opening is formed, it can consider as the side attachment wall of a taper configuration easily by using the wet etching method. Since degradation of EL layer resulting from a level difference will pose a remarkable problem if the side attachment wall of opening is not fully gently-sloping, cautions are required.
[0324] Next, continuation formation of the EL layer 5066 and the cathode (MgAg electrode) 5067 is carried out without carrying out atmospheric-air release using a vacuum deposition method. In addition, what is necessary is just to set to 180-300 [nm] (typically 200-250 [nm]) thickness whose thickness of the EL layer 5066 is 80-200 [nm] (typically 100-120 [nm]), and cathode 5067.
[0325] At this process, EL layer and cathode are formed one by one to the pixel corresponding to red, the pixel which corresponds green, and the pixel which corresponds blue. however, the ** which does not use a photolithography technique since EL layer is lacking in the resistance over a solution -- each color -- it must form individually. Then, it is desirable that hide except a desired pixel using a metal mask, and only a need part forms EL layer and cathode alternatively.
[0326] That is, the mask which hides except [all] the pixel corresponding to red first is set, and EL layer of red luminescence is alternatively formed using the mask. Subsequently, the mask which hides except [all] the pixel which corresponds green is set, and EL layer of green luminescence is alternatively formed using the mask. Subsequently, the mask which hides except [all] the pixel which corresponds blue similarly is set, and EL layer of blue luminescence is alternatively formed using the mask. In addition, the same mask may be used about although it has indicated that a mask which is altogether different here is used.
[0327] Although the method which forms three kinds of EL elements corresponding to RGB was used here, the method which combined the method which combined the EL element and color filter of white luminescence, blue, or the EL element and fluorescent substance (the color conversion layer of fluorescence: CCM) of bluish green luminescence, the method which puts the EL element corresponding to RGB on cathode (counterelectrode) using a transparent electrode may be used.
[0328] In addition, an ingredient well-known as an EL layer 5066 can be used. As a well-known

ingredient, when driver voltage is taken into consideration, it is desirable to use an organic material. For example, what is necessary is just to let 4 layer structures which become with a hole injection layer, an electron hole transportation layer, a luminous layer, and an electronic injection layer be EL layers.

[0329] Next, cathode 5067 is formed. In addition, although MgAg was used as cathode 5067 in this example, this invention is not limited to this. Other well-known ingredients may be used as cathode 5067.

[0330] The passivation film 5068 which becomes the last with a silicon nitride film is formed in the thickness of 300 [nm]. By forming the passivation film 5068, the EL layer 5066 can be protected from moisture etc. and the dependability of an EL element can be raised further. In addition, it is not necessary to necessarily form the passivation film 5068.

[0331] In this way, the luminescence equipment of structure as shown in drawing 23 (B) is completed. In addition, in the creation process of the luminescence equipment in this example, on the configuration of a circuit, and the relation of a process, although the gate signal line is formed by aluminum which is the wiring material which forms a source signal line and forms the source and a drain electrode by Ta and W which are the ingredient which forms the gate electrode, a different ingredient may be used.

[0332] By the way, by arranging TFT of the optimal structure not only for a picture element part but a drive circuit, the luminescence equipment of this example shows very high dependability, and its operating characteristic may also improve. Moreover, it is also possible to add metal catalysts, such as nickel, in a crystallization process, and to raise crystallinity. It is possible to carry out drive frequency of a source signal-line drive circuit by it more than 10 [MHz].

[0333] In addition, when completing to the condition of drawing 23 (B) in fact, airtightness is high and it is desirable to carry out packaging (enclosure) with few protection films (a laminate film, ultraviolet-rays hardening resin film, etc.) of degasifying or the sealing material of translucency so that it may not be further put to the open air. In that case, if the interior of a sealing material is made into an inert atmosphere or a hygroscopic material (for example, barium oxide) is arranged inside, the dependability of an EL element will improve.

[0334] Moreover, if processing of packaging etc. raises airtightness, the connector (flexible print circuit: FPC) for connecting the terminal and external signal terminal which were taken about from the component formed on the substrate or the circuit will be attached.

[0335] Moreover, if the process shown by this example is followed, the number of photo masks required for production of luminescence equipment can be stopped. Consequently, a process can be shortened and it can contribute to reduction of a manufacturing cost, and improvement in the yield.

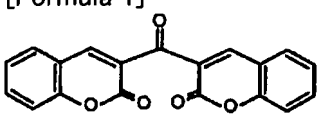
[0336] It combines with examples 1-8 freely, and this example can be carried out.

[0337] (Example 10) In this invention, external luminescence quantum efficiency can be raised by leaps and bounds by using EL ingredient which can use the phosphorescence from a triplet exciton for luminescence. Thereby, low-power-izing of an EL element, reinforcement, and lightweight-ization are attained.

[0338] Here, a triplet exciton is used and the report which raised external luminescence quantum efficiency is shown. [(T. Tsutsui, C.Adachi, S.Saito, Photochemical Processes in Organized Molecular Systems, ed.KHonda (Elsevier Sci.Pub., Tokyo, 1991), p.437.) 0339] The molecular formula of EL ingredient (coumarin coloring matter) reported by the above-mentioned paper is shown below.

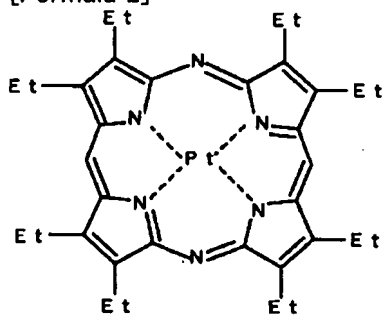
[0340]

[Formula 1]

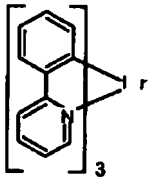


[0341] [(M. A.Baldo, D.F.O'Brien, Y.You, A.Shoustikov, S.Sibley, M.E.Thompson, S.R.Forrest, Nature 395 (1998) p.151.) 0342] The molecular formula of EL ingredient (Pt complex) reported by the above-mentioned paper is shown below.

[0343]
[Formula 2]



[0344] It Lamansk(ies). M. — A.Baldo and S. — P. E.Burrrows and M.E.Thompson, S. — R.Forrest, Appl.Phys.Lett., and 75 (1999) p.4. (it Watanabe(s) T. — Tsutsui, M.-J.Yang, M.Yahiro, KNakamura, and T. —) T. (1999) tsuji, Y.Fukuda, T.Wakimoto, S.Mayaguchi, Jpn.Appl.Phys., 38 (12B) L1502. [0345] The molecular formula of EL ingredient (Ir complex) reported by the above-mentioned paper is shown below.
[0346]
[Formula 3]



[0347] If phosphorescence luminescence from a triplet exciton can be used as mentioned above, implementation of one 3 to 4 times the high external luminescence quantum efficiency of this will be attained from the case where the firefly luminescence from a singlet exciton is used theoretically.
[0348] In addition, it combines with any configuration of an example 1 - an example 9 freely, and the configuration of this example can be carried out.
[0349] (Example 11) This example explains the case where an organic semiconductor is used for a barrier layer, as TFT used for the luminescence equipment of this invention. in addition, TFT which used the organic semiconductor for the barrier layer hereafter -- organic -- it is referred to as TFT.
[0350] drawing 27 (A) -- organic [of a planar mold] -- the sectional view of TFT is shown. The gate electrode 8002 is formed on the substrate 8001. And the gate electrode 8002 is covered and gate dielectric film 8003 is formed on the substrate 8001. Moreover, the source electrode 8005 and the drain electrode 8006 are formed on gate dielectric film 8003. Furthermore, the source electrode 8005 and the drain electrode 8006 are covered, and the film (organic-semiconductor film) 8004 which consists of an organic semiconductor is formed on gate dielectric film 8003.
[0351] drawing 27 (B) — organic [of a reverse stagger mold] -- the sectional view of TFT is shown. The gate electrode 8102 is formed on the substrate 8101. And the gate electrode 8102 is covered and gate dielectric film 8103 is formed on the substrate 8101. Moreover, the organic-semiconductor film 8104 is formed on gate dielectric film 8103. Furthermore, the source electrode 8105 and the drain electrode 8106 are formed on the organic-semiconductor film 8104.

[0352] drawing 27 (C) -- organic [of a stagger mold] — the sectional view of TFT is shown. The source electrode 8205 and the drain electrode 8106 are formed on the substrate 8201. And the source electrode 8205 and the drain electrode 8106 are covered, and the organic-semiconductor film 8204 is formed on the substrate 8201. Moreover, gate dielectric film 8203 is formed on the organic-semiconductor film 8204. Furthermore, the gate electrode 8202 is formed

on gate dielectric film 8203.
[0353] An organic semiconductor is classified into a macromolecule system and a low-molecular system. As for the typical ingredient of a giant-molecule system, the poly thiophene, polyacethylene, Pori (N-methyl pyrrole), Pori (3-alkyl thiophene), the poly propine vinylene, etc. are mentioned.
[0354] The organic-semiconductor film which has the poly thiophene can be formed with an electric-field polymerization method or a vacuum deposition method. The organic-semiconductor film which has polyacethylene can be formed by the chemistry polymerization method or the applying method. The organic-semiconductor film which has Pori (N-methyl pyrrole) can be formed by the chemistry polymerization method. The organic-semiconductor film which has Pori (3-alkyl thiophene) can be formed by the applying method or the LB method. The organic-semiconductor film which has the poly propine vinylene can be formed by the applying method.
[0355] Moreover, as for the typical ingredient of a low-molecular system, a quarter thiophene, a dimethyl quarter thiophene, JIFUTARO cyanine, an anthracene, tetracene, etc. are mentioned. The organic-semiconductor film using the ingredient of these low-molecular system can mainly be formed by vacuum deposition and the cast which used the solvent.
[0356] The configuration of this example can be combined with the configuration and freedom of examples 1-10, and can be carried out.
[0357] (Example 12) Since the luminescence equipment using an EL element is a spontaneous light type, compared with a liquid crystal display, it is excellent in the visibility in a bright location, and its angle of visibility is large. Therefore, it can use for the display of various electronic equipment.
[0358] As electronic equipment using the luminescence equipment of this invention, a video camera, a digital camera, A goggles mold display (head mount display), a navigation system, Sound systems (a car audio, audio component stereo, etc.), a note type personal computer, A game device, a Personal Digital Assistant (a mobile computer, a cellular phone, a handheld game machine, or digital book), The picture reproducer (equipment equipped with the display which specifically reproduces record media, such as Digital Versatile Disc (DVD), and can display the image) equipped with the record medium etc. is mentioned. Since importance is attached to the size of an angle of visibility, as for especially the Personal Digital Assistant with many opportunities to see a screen from across, it is desirable to use luminescence equipment. The example of these electronic equipment is shown in drawing 24 .
[0359] Drawing 24 (A) is EL display and contains a case 2001, susceptor 2002, a display 2003, the loudspeaker section 2004, and video input terminal 2005 grade. The luminescence equipment of this invention can be used for a display 2003. Since it is a spontaneous light type, luminescence equipment has an unnecessary back light, and it can be made into a display thinner than a liquid crystal display. In addition, as for EL display, all the displays for information displays the object for personal computers, the object for TV broadcast reception, for an advertising display, etc. are contained.
[0360] Drawing 24 (B) is a digital still camera, and contains a body 2101, a display 2102, the television section 2103, the actuation key 2104, the external connection port 2105, and shutter 2106 grade. The luminescence equipment of this invention can be used for a display 2102.
[0361] Drawing 24 (C) is a note type personal computer, and contains a body 2201, a case 2202, a display 2203, a keyboard 2204, the external connection port 2205, and pointing mouse 2206 grade. The luminescence equipment of this invention can be used for a display 2203.
[0362] Drawing 24 (D) is a mobile computer and contains a body 2301, a display 2302, a switch 2303, the actuation key 2304, and infrared port 2305 grade. The luminescence equipment of this invention can be used for a display 2302.
[0363] Drawing 24 (E) is the picture reproducer (specifically DVD regenerative apparatus) of the pocket mold equipped with the record medium, and contains a body 2401, a case 2402, a display A2403, a display B2404, the record-media (DVD etc.) reading section 2405, the actuation key 2406, and loudspeaker section 2407 grade. although a display A2403 mainly displays image information and a display B2404 mainly displays text -- the luminescence equipment of this invention -- these displays A and B -- it can use for 2403 and 2404. In addition, a home video

game machine machine etc. is contained in the picture reproducer equipped with the record medium.

[0364] Drawing 24 (F) is a goggles mold display (head mount display), and contains a body 2501, a display 2502, and the arm section 2503. The luminescence equipment of this invention can be used for a display 2502.

[0365] Drawing 24 (G) is a video camera and contains a body 2601, a display 2602, a case 2603, the external connection port 2604, the remote control receive section 2605, the television section 2606, a dc-battery 2607, the voice input section 2608, and actuation key 2609 grade. The luminescence equipment of this invention can be used for a display 2602.

[0366] Drawing 24 (H) is a cellular phone and contains a body 2701, a case 2702, a display 2703, the voice input section 2704, the voice output section 2705, the actuation key 2706, the external connection port 2707, and antenna 2708 grade here. The luminescence equipment of this invention can be used for a display 2703. In addition, a display 2703 can stop the power consumption of a cellular phone by displaying a white alphabetic character on a black background.

[0367] In addition, if the luminescence brightness of EL ingredient will become high in the future, it will also become possible to carry out expansion projection of the light containing the outputted image information with a lens etc., and to use for the projector of a front mold or a rear mold.

[0368] Moreover, the above-mentioned electronic equipment displays more often the information distributed through electronic communication lines, such as the Internet and CATV (cable television), and its opportunity to display especially animation information has been increasing. Since the speed of response of EL ingredient is very high, luminescence equipment is desirable to a movie display.

[0369] Moreover, in order that the part which is emitting light may consume power, as for luminescence equipment, it is desirable to display information that the amount of light-emitting part decreases as much as possible. Therefore, when using luminescence equipment for the display which is mainly concerned with text like a Personal Digital Assistant especially a cellular phone, or a sound system, it is desirable to drive so that text may be formed by part for a light-emitting part by making a nonluminescent part into a background.

[0370] As mentioned above, the applicability of this invention is very wide, and using for the electronic equipment of all fields is possible. Moreover, the electronic equipment of this example may use the luminescence equipment of which configuration shown in examples 1-11.

[0371]

[Effect of the Invention]

[0372] By the configuration mentioned above, the luminescence equipment of this invention can obtain fixed brightness, without being influenced by the temperature change. Moreover, in color display, even when the EL element which has a different EL ingredient for every color is prepared, the brightness of the EL element of each color can prevent changing scatteringly and not obtaining a desired color with temperature.

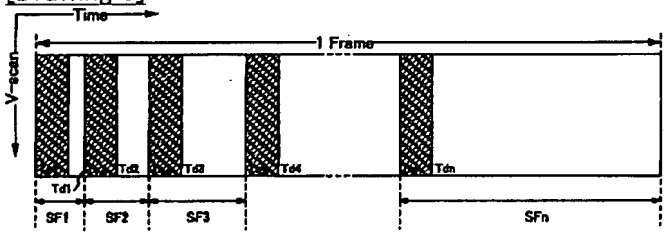
[Translation done.]

* NOTICES *

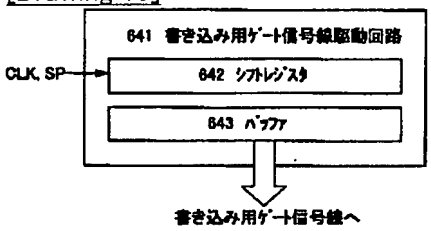
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

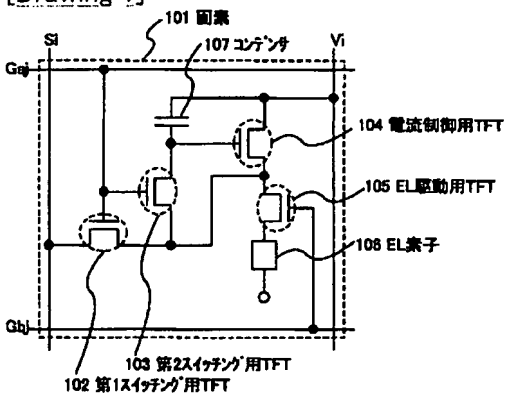
[Drawing 5]



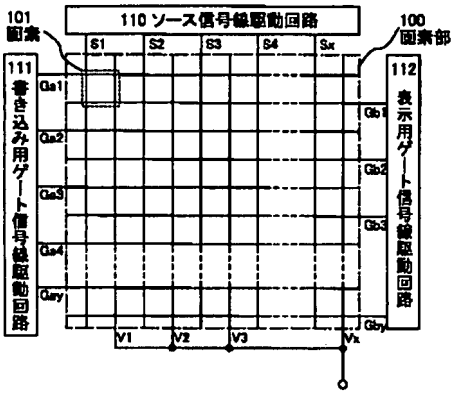
[Drawing 19]



[Drawing 1]

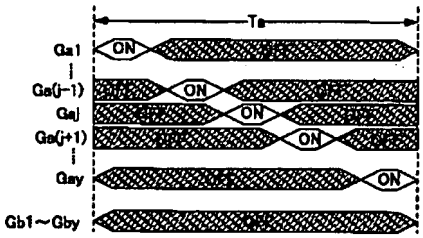


[Drawing 2]

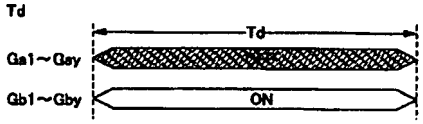


[Drawing 3]

(A)書き込み期間 Ta

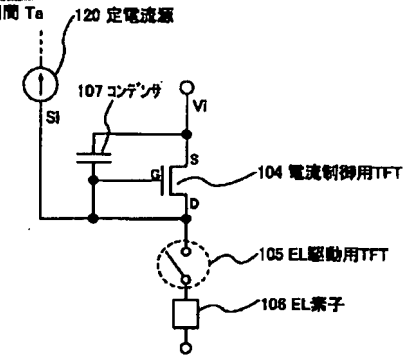


(B)表示期間 Td

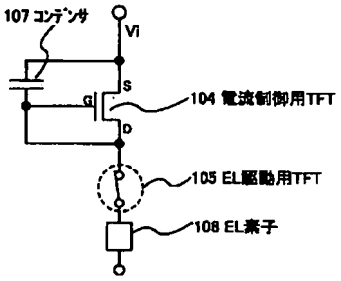


[Drawing 4]

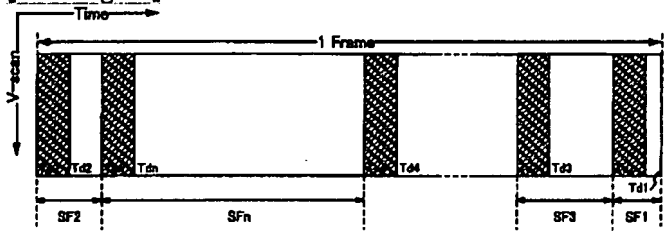
(A)書き込み期間 Ta



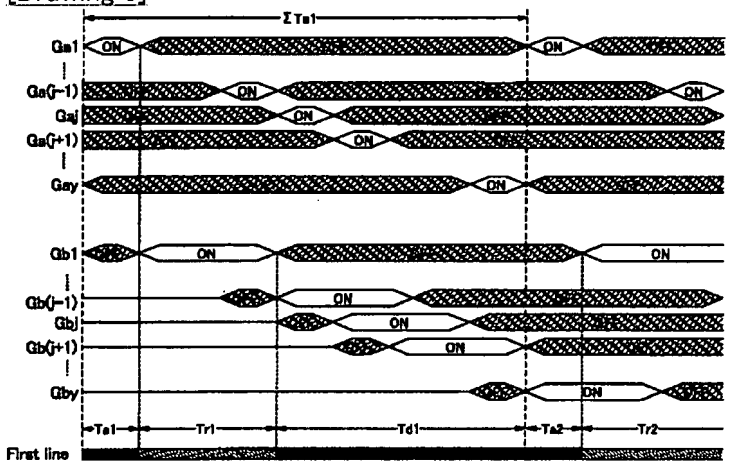
(B)表示期間 Td



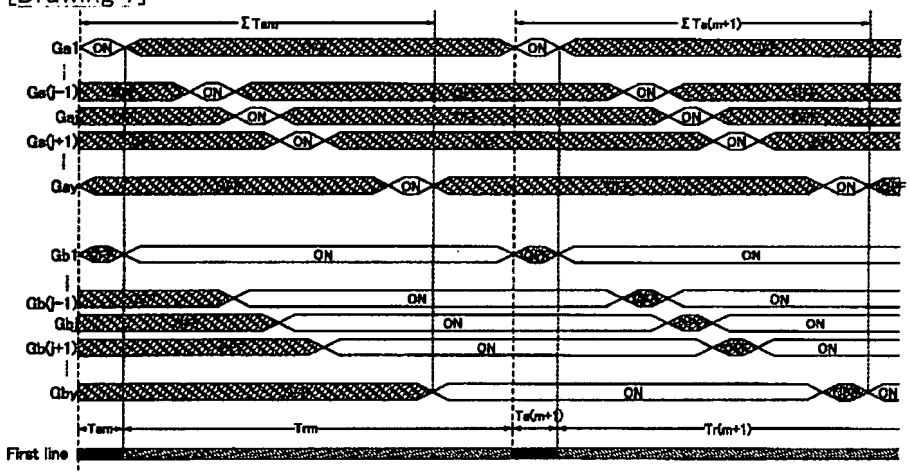
[Drawing 10]



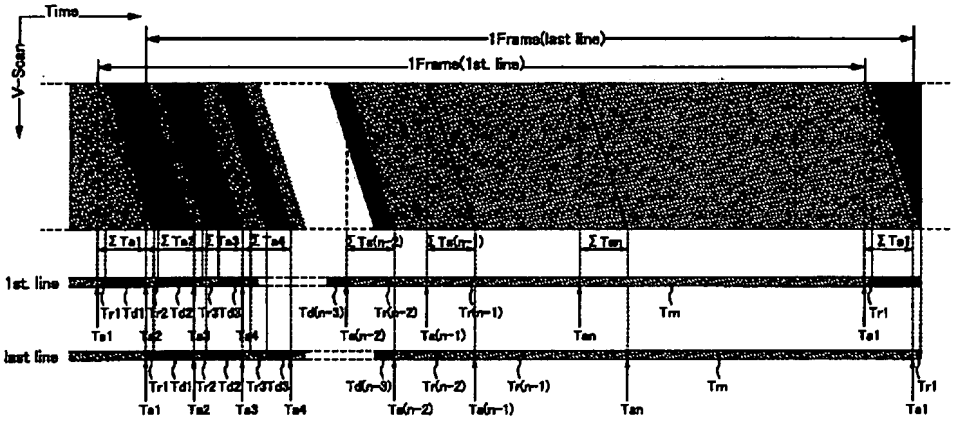
[Drawing 6]



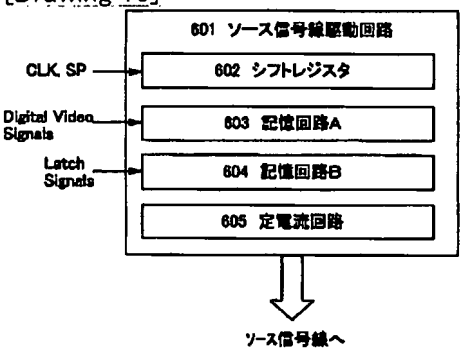
[Drawing 7]



[Drawing 9]

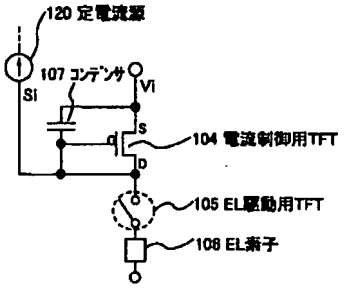


[Drawing 16]

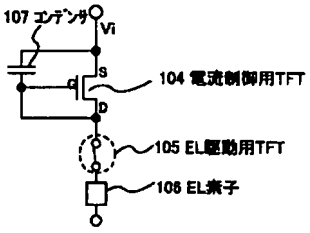


[Drawing 8]

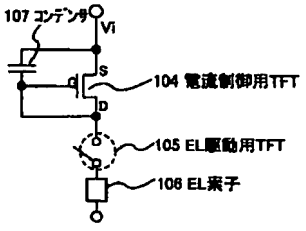
(A)書き込み期間Ta(Ga選択、Gb非選択)



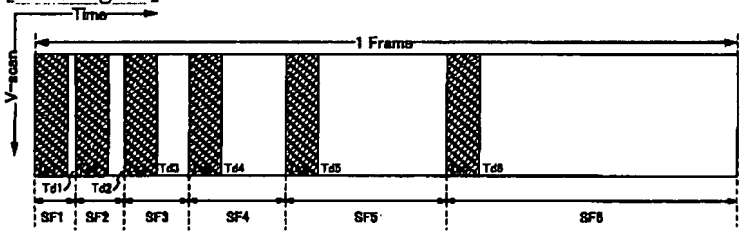
(B)表示期間Tr(Ga非選択、Gb選択)



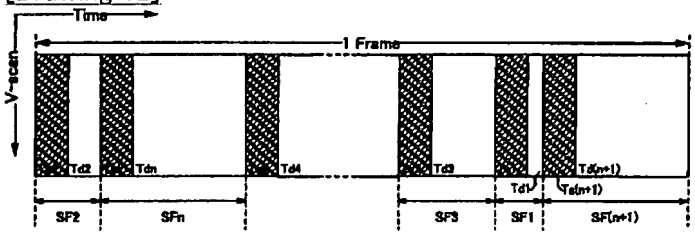
(C)非表示期間Te(Ga非選択、Gb非選択)



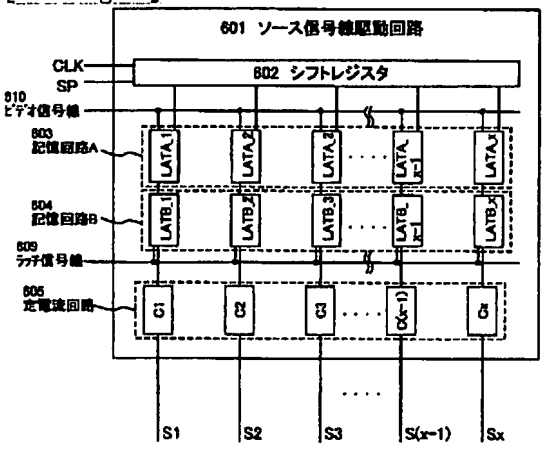
[Drawing 11]



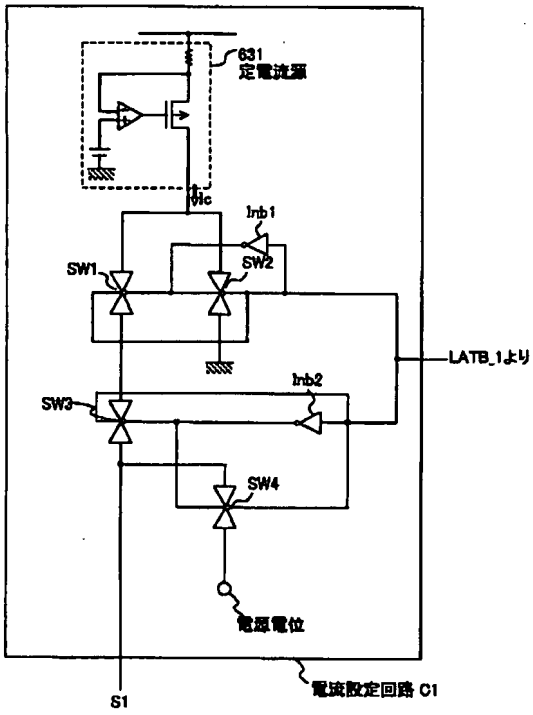
[Drawing 12]



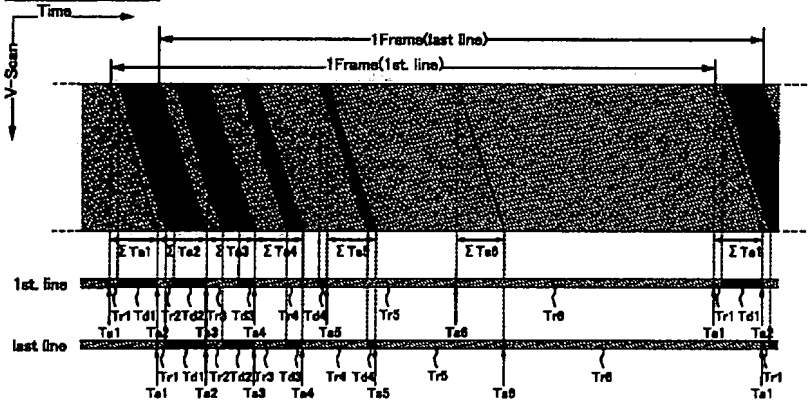
[Drawing 17]



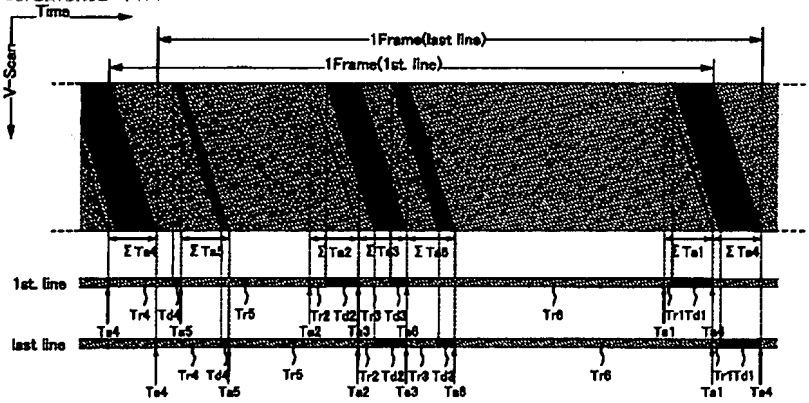
[Drawing 18]



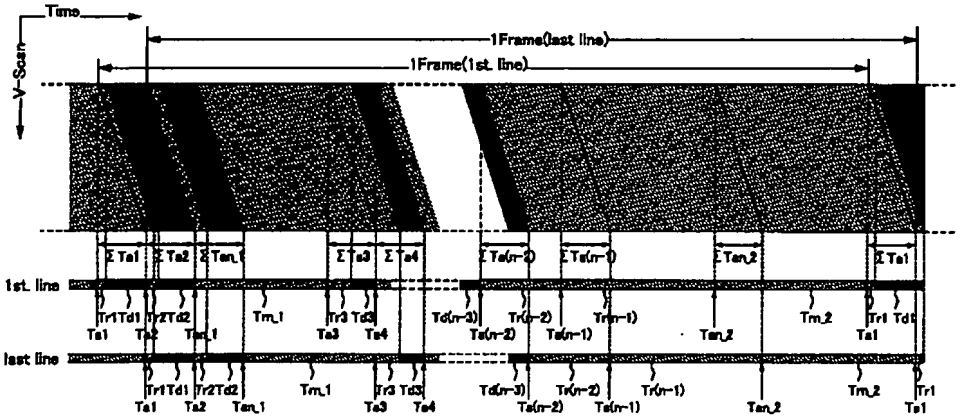
[Drawing 13]



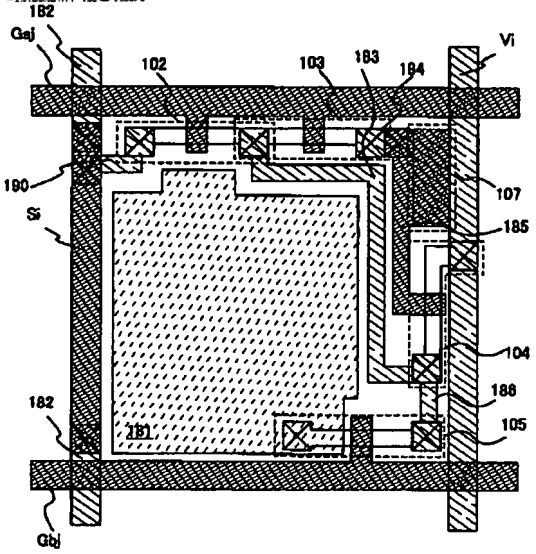
[Drawing 14]



[Drawing 15]

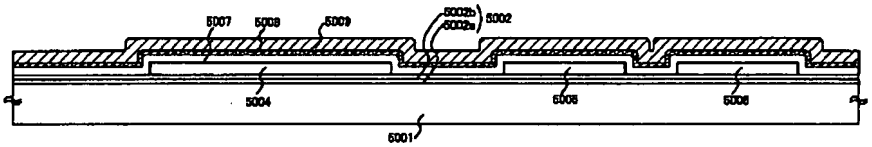


[Drawing 20]

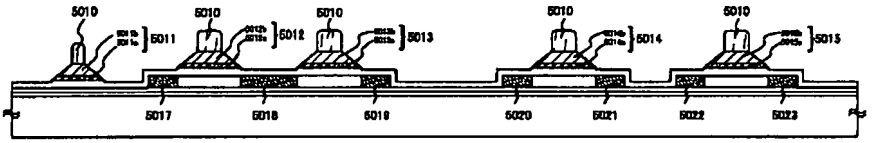


[Drawing 21]

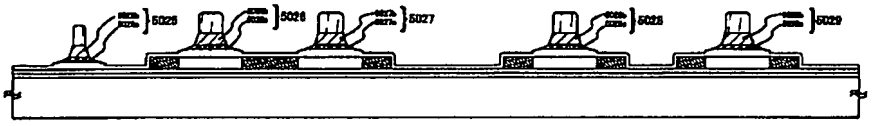
(A) 島状半導体層，ゲート絶縁膜，ゲート電極用第1・第2の導電膜の形成



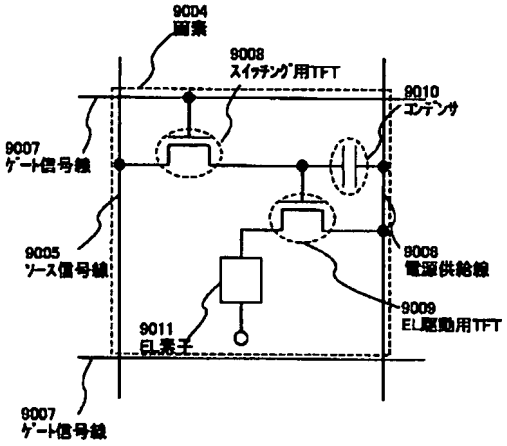
(B) 第1のエッチング処理，第1のドーピング処理



(C) 第2のエッチング処理

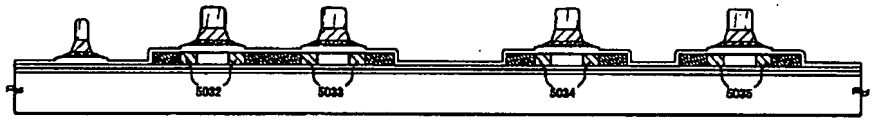


[Drawing 25]

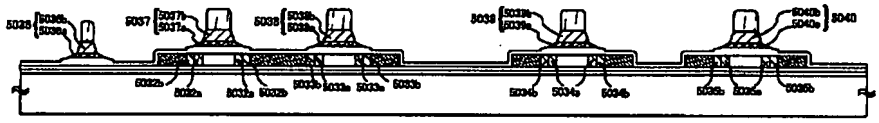


[Drawing 22]

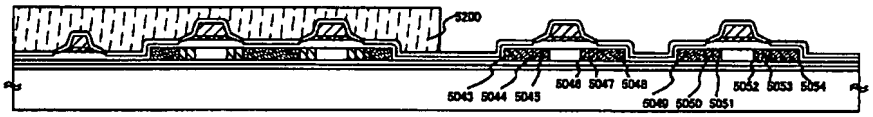
(A) 第2のドーピング処理



(B) 第3のエッチング処理

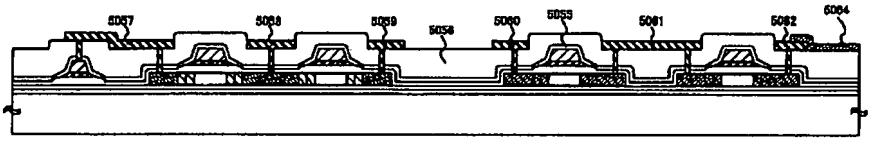


(C) 第3のドーピング処理

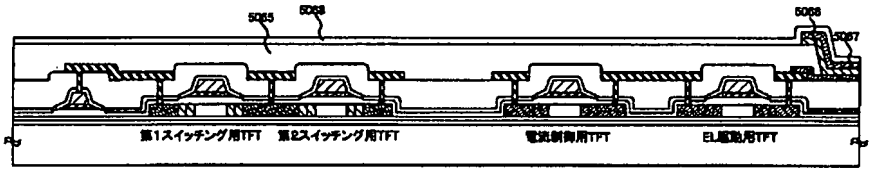


[Drawing 23]

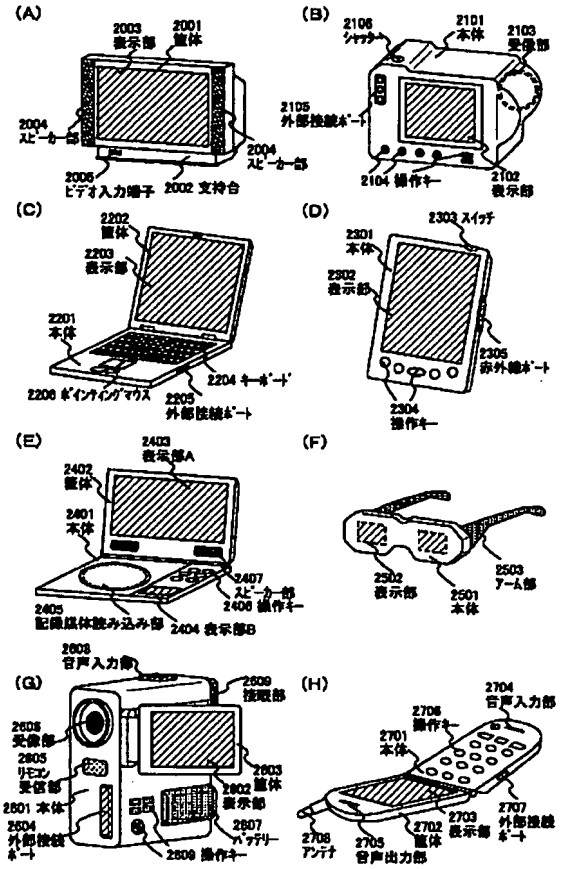
(A) 第1，第2の層間絶縁膜，配線，画素電極形成



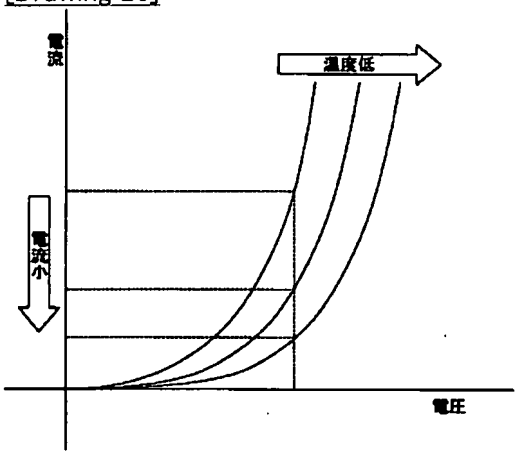
(B) 第3の層間絶縁膜，EL層，陰極電極，パッシベーション膜形成



[Drawing 24]

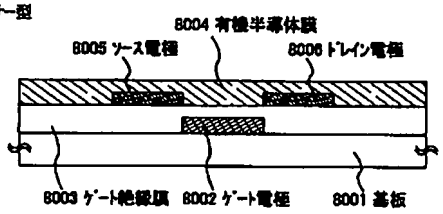


[Drawing 26]

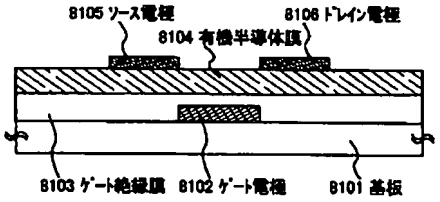


[Drawing 27]

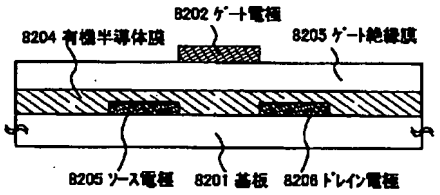
(A)プレーナー型



(B)逆スタガー型



(C)スタガー型



[Translation done.]